

Compal Confidential

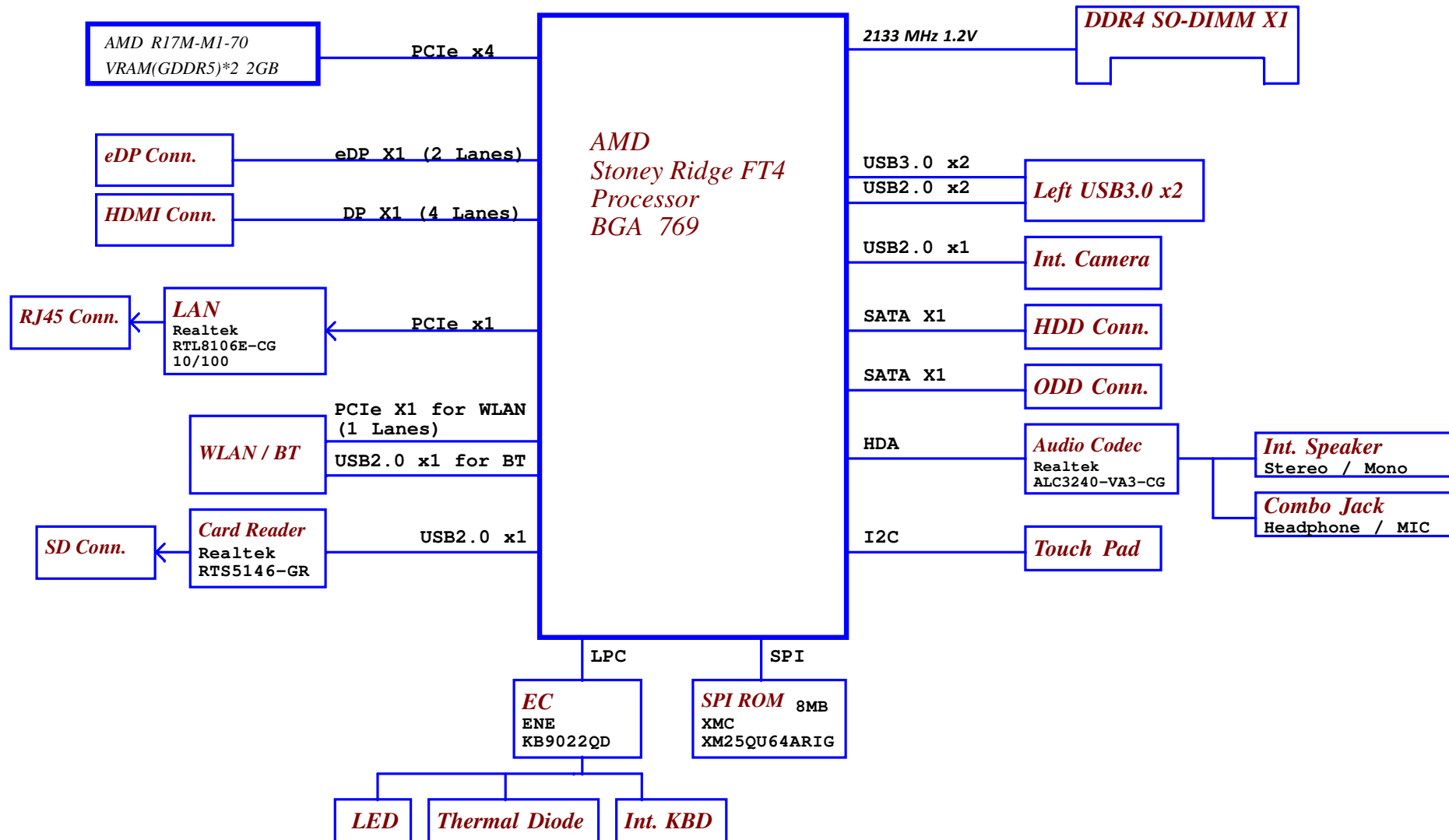
DIS M/B Schematics Document

AMD Stoney Ridge FT4

LA-G241P
2018-03-12
REV : 1 . 0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2018/03/12	Deciphered Date	2019/03/12	
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AMD Stoney Ridge FT4



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Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	ON	ON
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+2.5V	2.5V switched power rail for DDR	ON	ON	OFF
+0.6V	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVBATT	RTC power	ON	ON	ON
+0.775VALW	0.775V always on power rail	ON	ON	ON

	SOURCE	APU	BATT	NPCE388N	SO-DIMM	WLAN	Thermal Sensor
EC_SMB_CK1 EC_SMB_DA1	ENE9022 +3VL	X	V +3VALW	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	X	X
EC_SMB_CK2 EC_SMB_DA2	ENE9022 +3VS	V +1.8VS	X	X	X	X	V +3VS

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011x b	16H	APU	1001 100X b	98H
Charger	0001 0010 b	12H			

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000X b	A0H	GPU	0100 0001 b	0X41H

Port	Device
0	LAN
1	
2	WLAN
3	

USB 3.0	USB 2.0	3 External USB Port
	0	
	1	WLAN/BT Combo
	2	Camera
	3	Card Reader
	4	
1	5	Left USB3.0 port 1
2	6	Left USB3.0 port 2
	7	

OC#	USB Port	
0		
1	USB2 port5	USB3 port1
2		
3		

UC1 A9 9425s

A9 9425 R3
SA0000BGS20

X4EABS38L51

ZZZ 45@

HDMI Logo
R00000003HM

UC1 A6 9225@

A6-9225 R3
SA0000BGT20

UC1 A4 9125@

A4 9125 R3
SA0000BM510

ZZZ Dmyf

PCB DLADE I
DAZ29700101

UC1 E2 9000@

E2 9000 R3
SA00009W810

PCB DLADE I
DAZ29700201

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VAL#	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

[illegible]

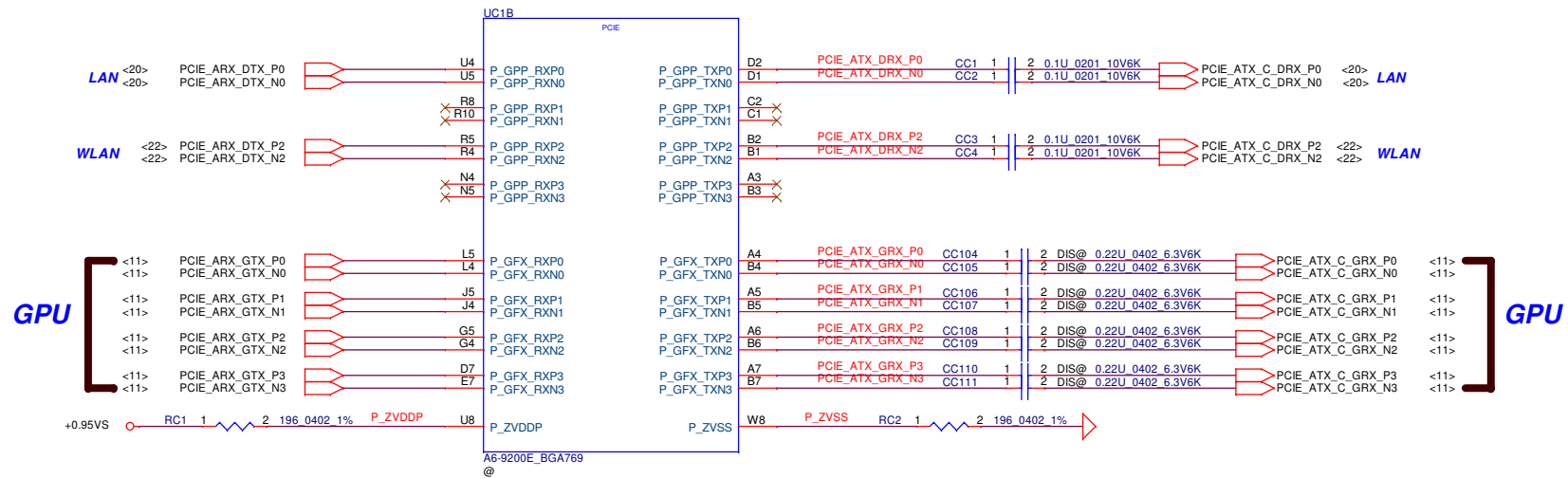
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PCB DLADE LA-G241P LS-G201P/G202P 02
DAZ29700101

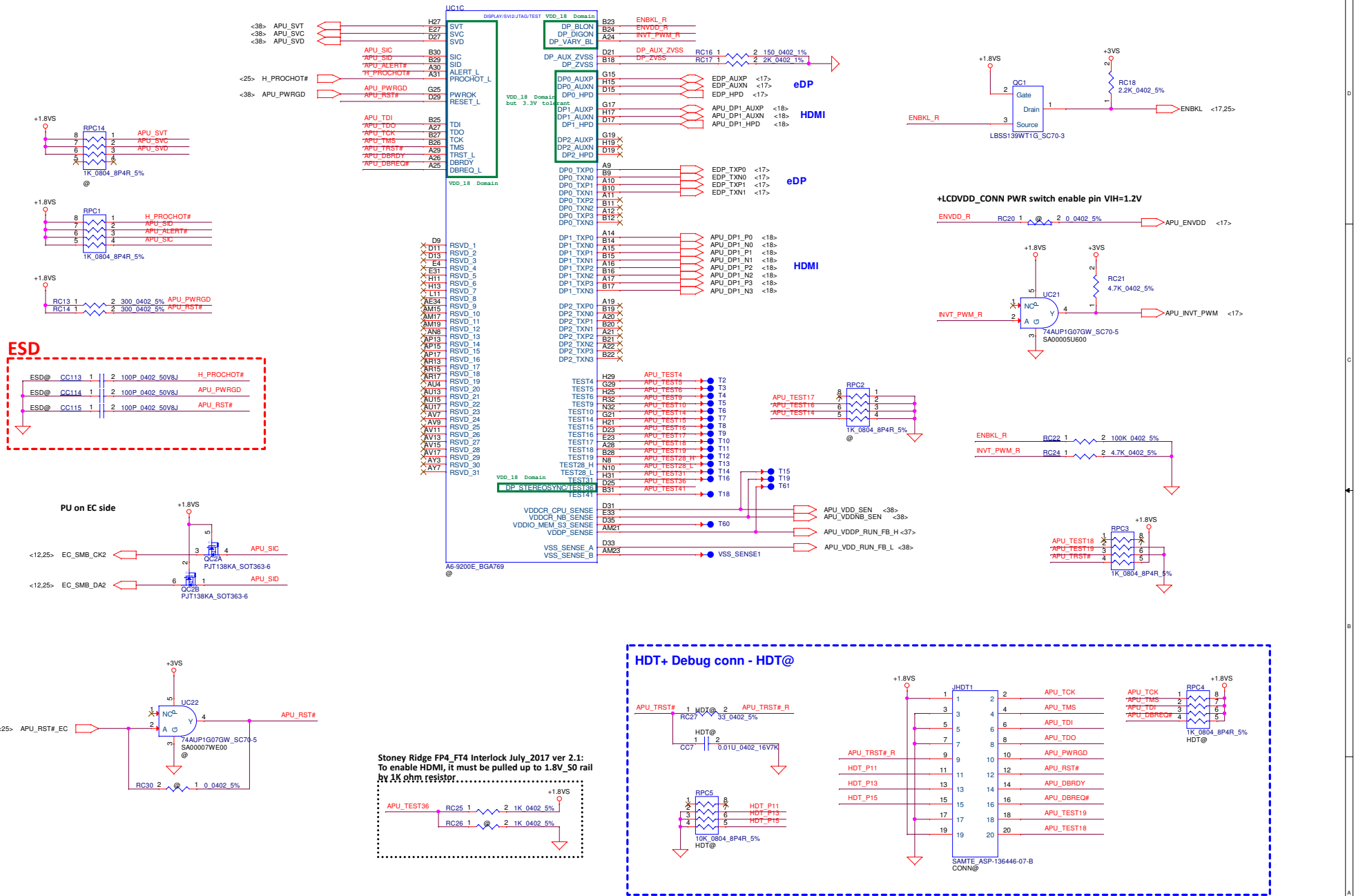
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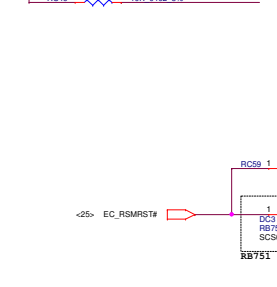
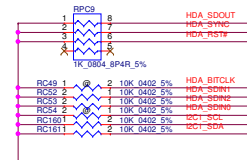
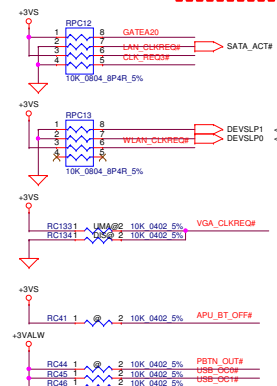
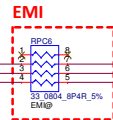
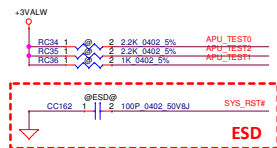
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				Date:	Monday, March 12, 2018	

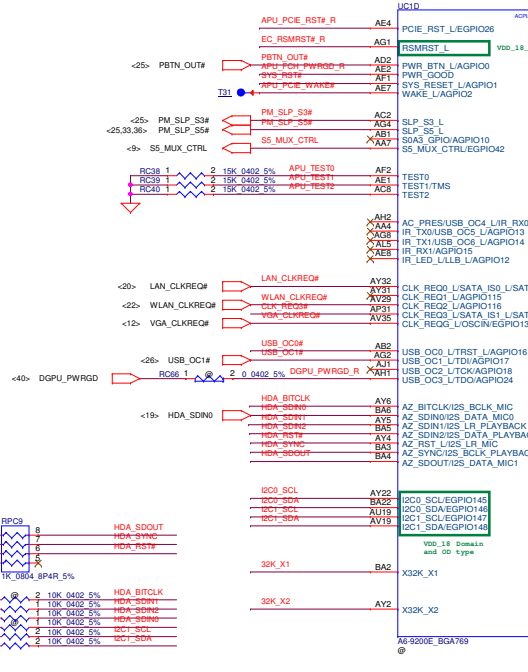
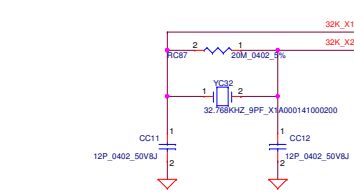


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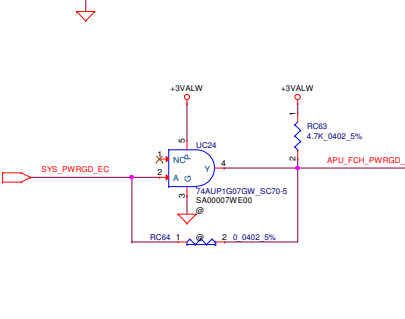
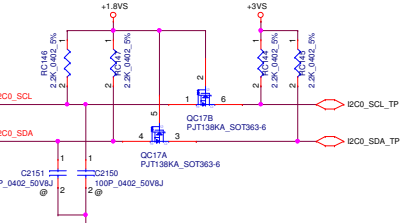




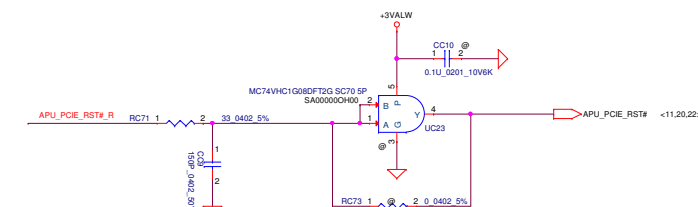
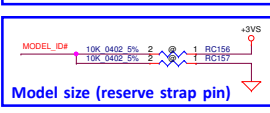
32.768KHz CRYSTAL



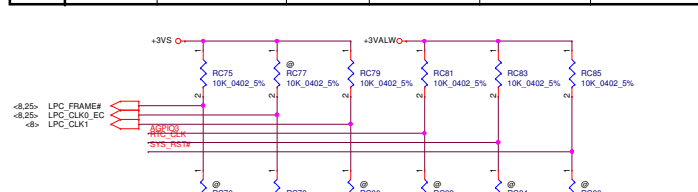
I2C Port 0: Touch Pad

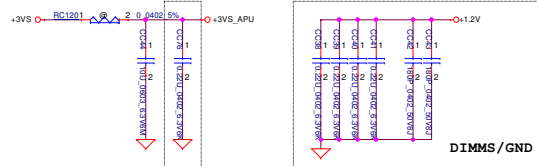
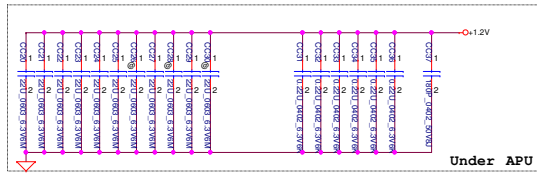


Function	Detect
ODD	0
2nd HDD	1

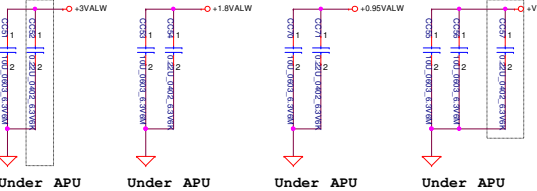
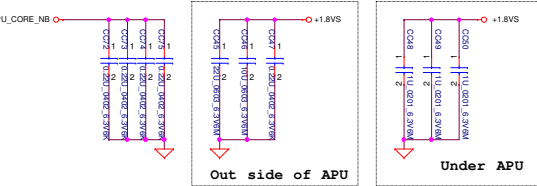


	LPC_CLK0_EC	LPC_CLK1	LPC_FRAME#	AGPIO3 <INT PU>	RTC_CLK <INT PU>	SYS_RST# <INT PU>
H	BOOT FAIL TIMER ENABLED	Use 48MHz crystal CLK and generate both internal and external CLK (DEFAULT)	SPI ROM (DEFAULT)	ENHANCED RESET LOGIC (for quicker SS resume) (DEFAULT)	COIN BATT ON BOARD (DEFAULT)	NORMAL RESET MODE (DEFAULT)
L	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100MHz PCIe CLK as reference CLK and generate internal CLK only	LPC ROM	TRADITION RESET	COIN BATT NOT ON BOARD	SHORT RST MODE

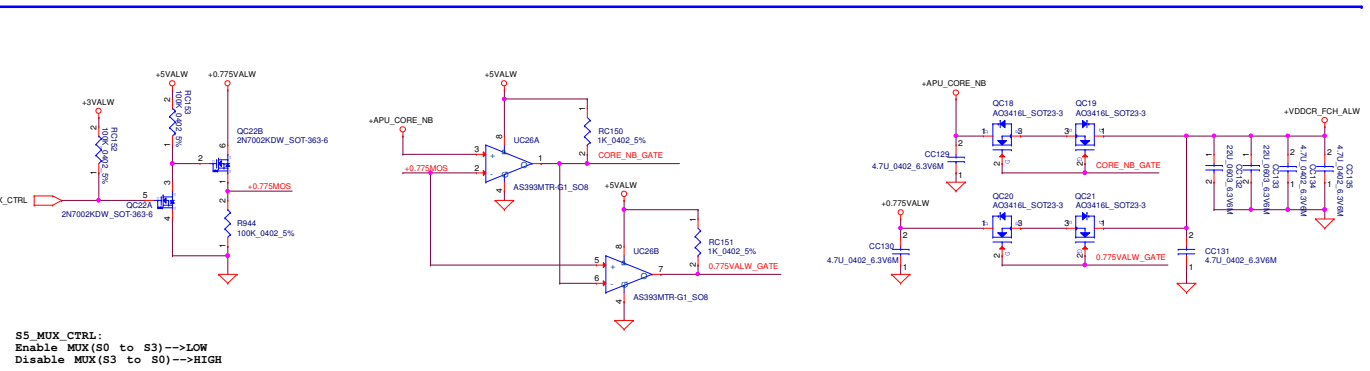
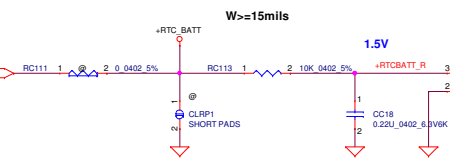
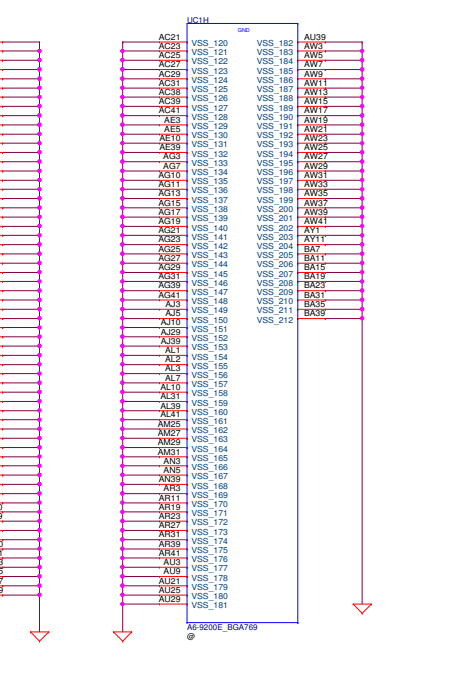
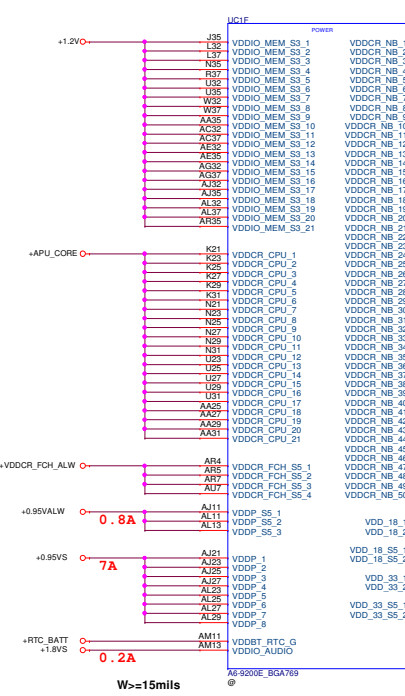
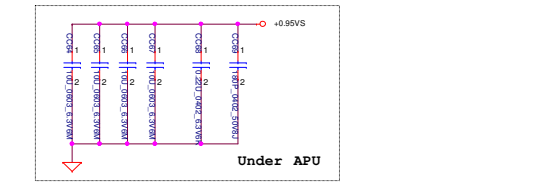
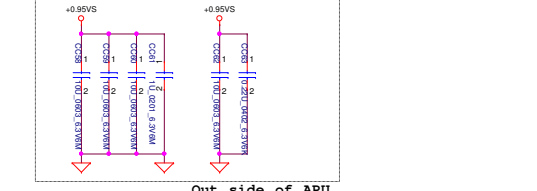




Under APU ACROSS +1.2V_VDDQ AND VSS SPLITT

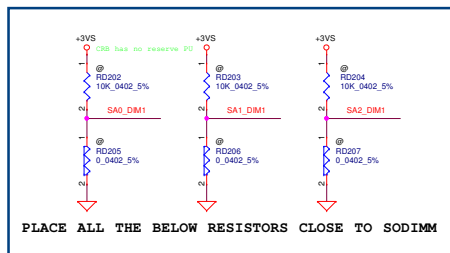


+0.95VS OF APU

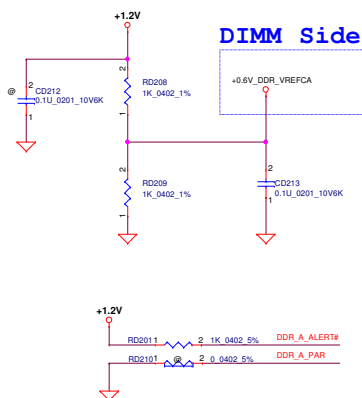


S5_MUX_CTRL:
Enable MUX (S0 to S3)--->LOW
Disable MUX (S3 to S0)--->HIGH

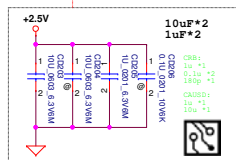
Stoney So-DIMM1



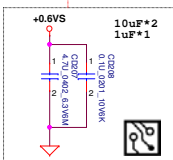
SPD ADDRESS FOR CHANNEL A :
SA0 = 0; SA1 = 0; SA2 = 0.



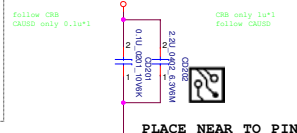
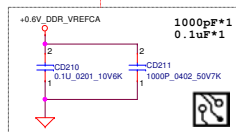
Layout Note:
Place near JDIMM1.257,259



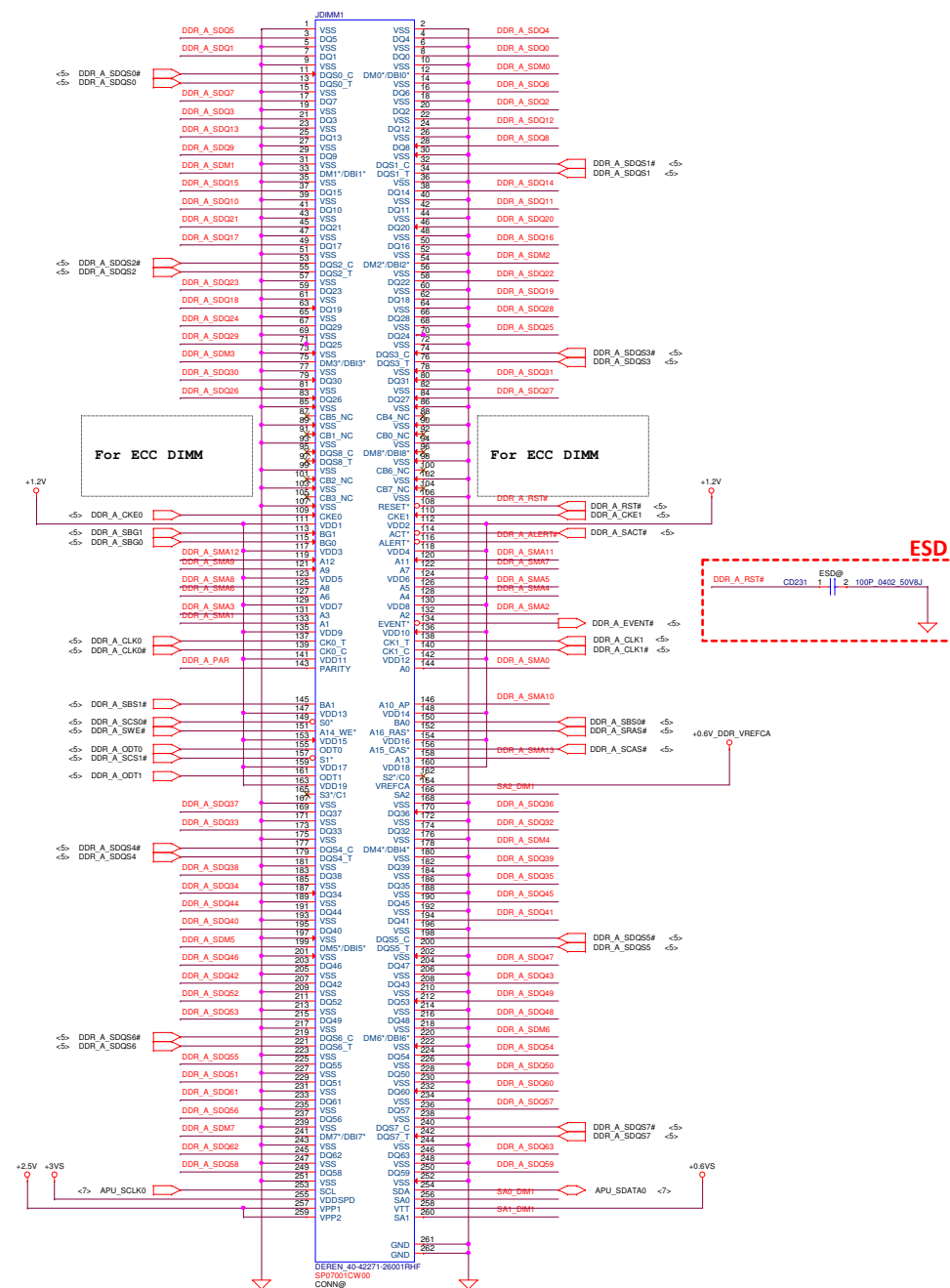
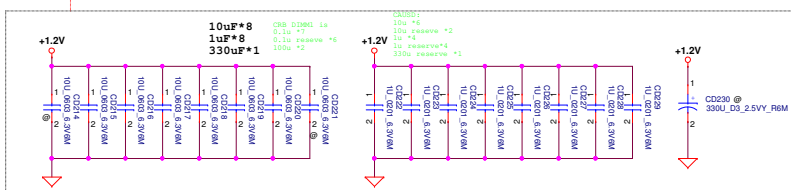
Layout Note:
Place near JDIMM1.258

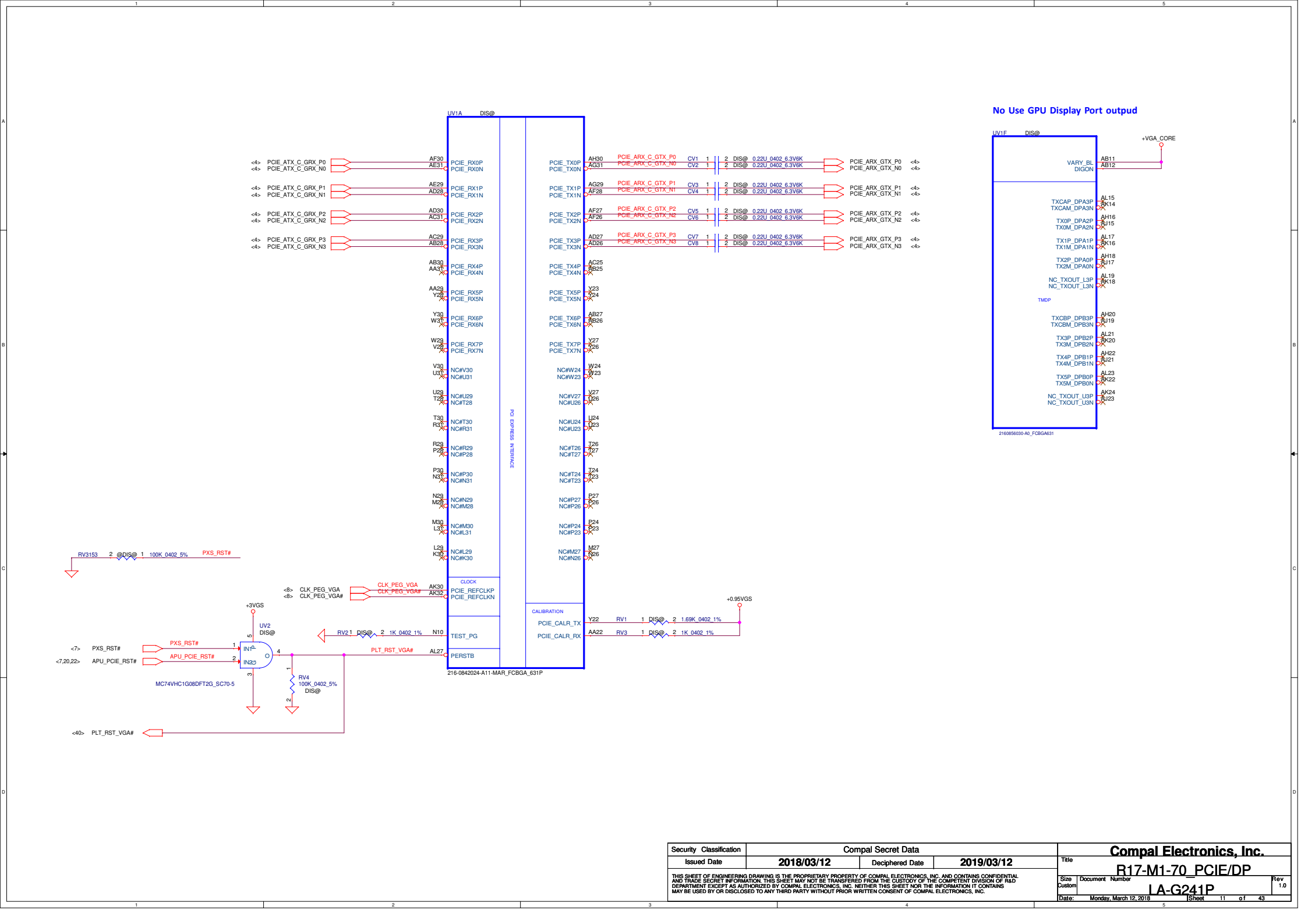


Layout Note:
PLACE THE CAP near JDIMM1. 164

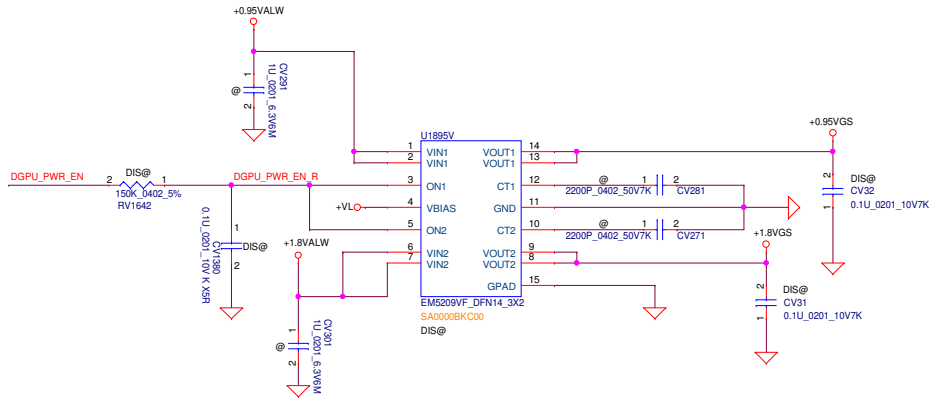


Layout Note:
Place near JDIMM1

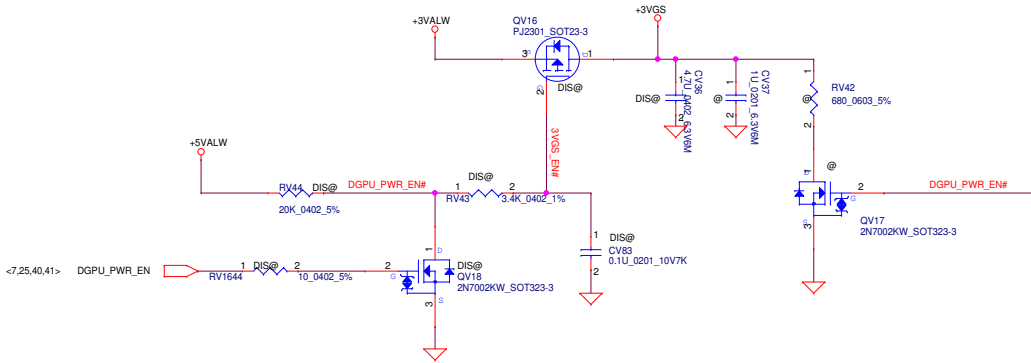




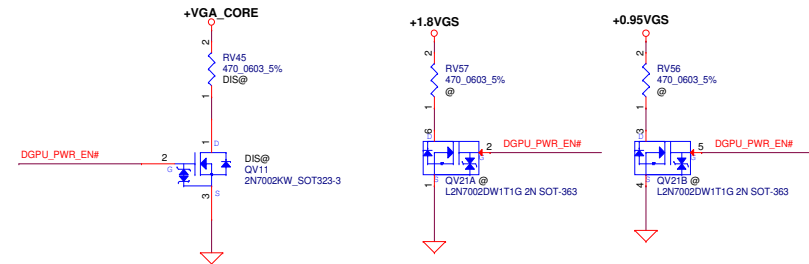
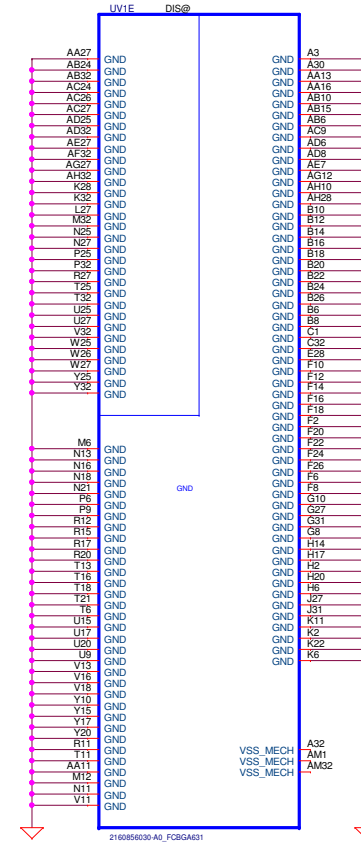
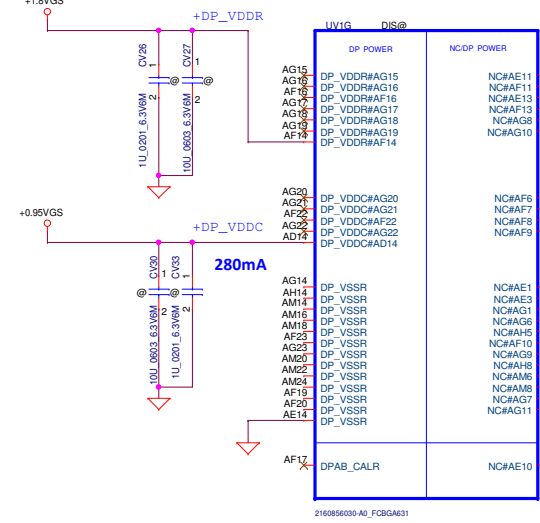
**+1.8VALW TO +1.8VGS
+0.95VALW TO +0.95VGS
Load switch**



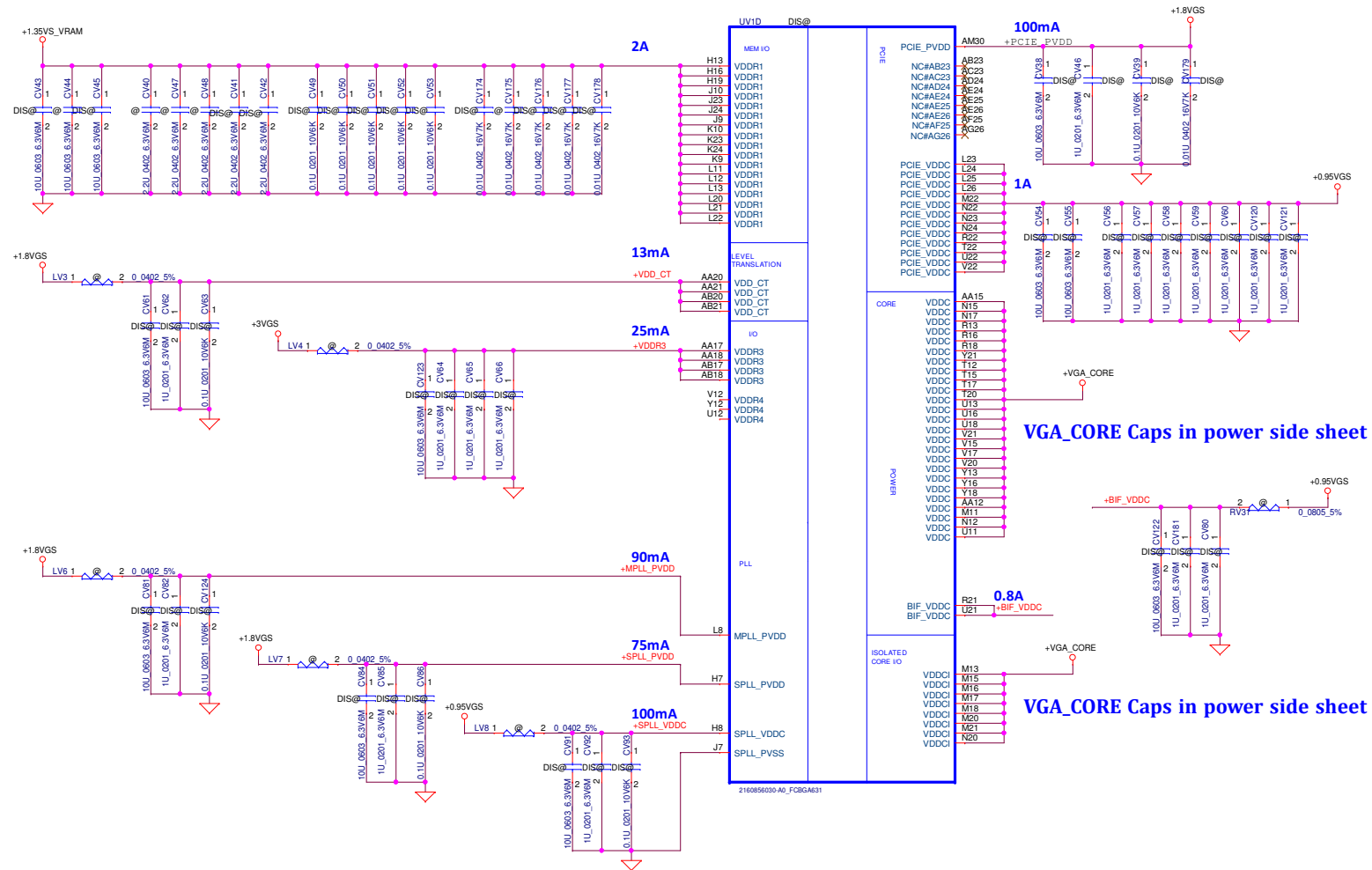
+3VALW to +3VGS



No Use GPU Display Port output

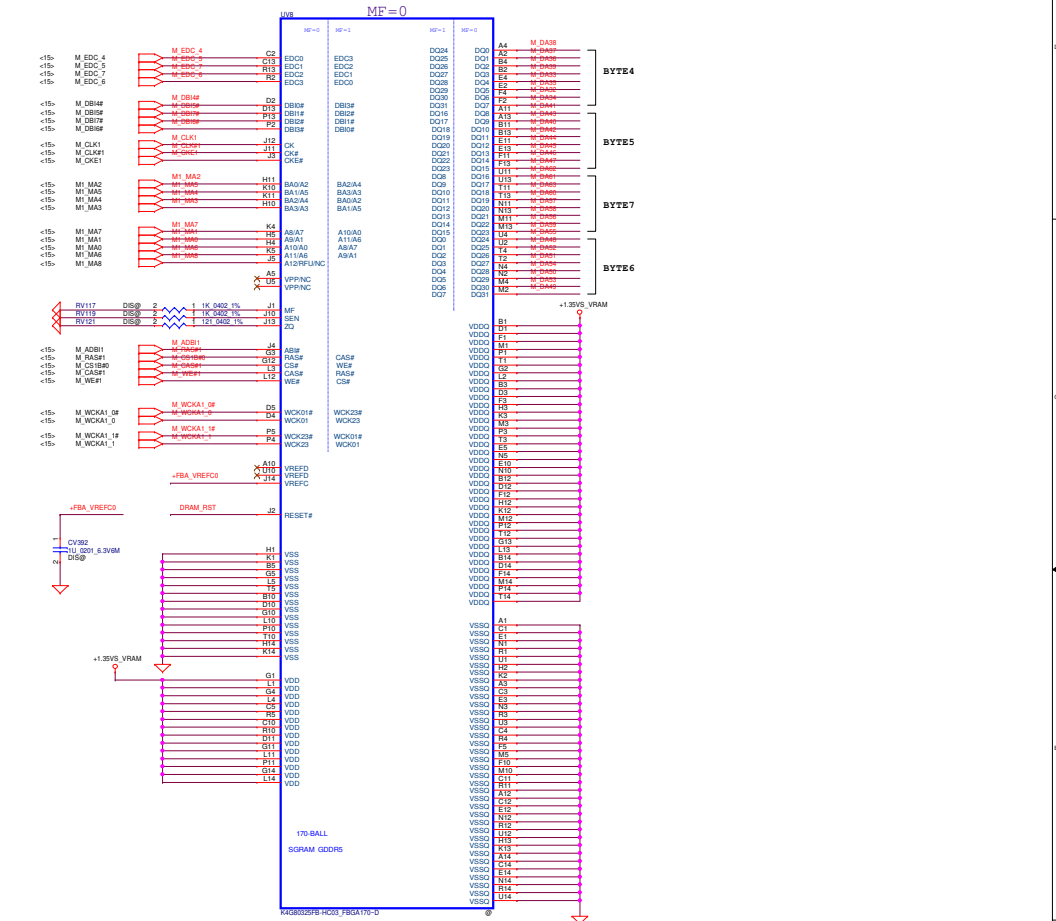
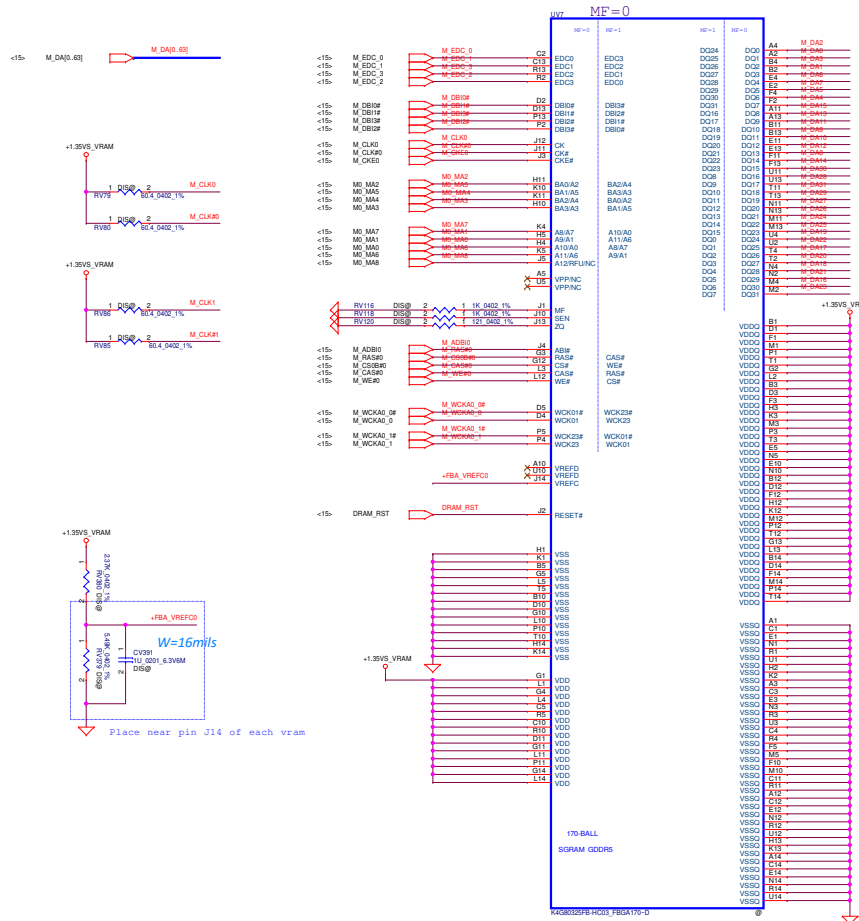


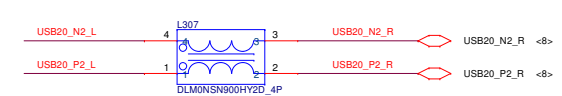
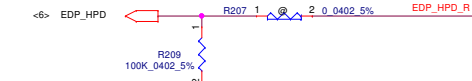
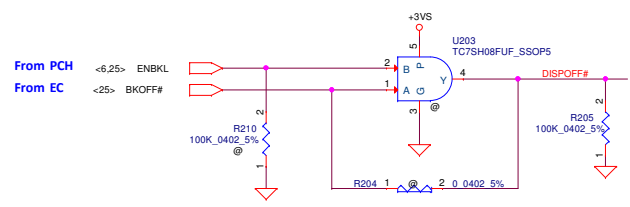
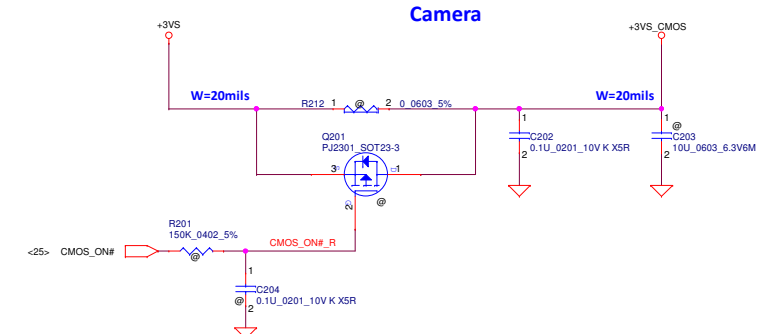
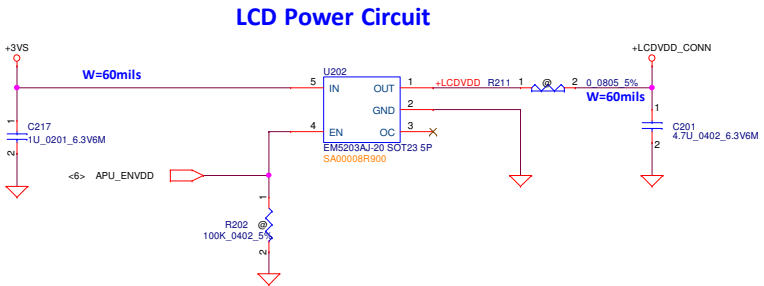
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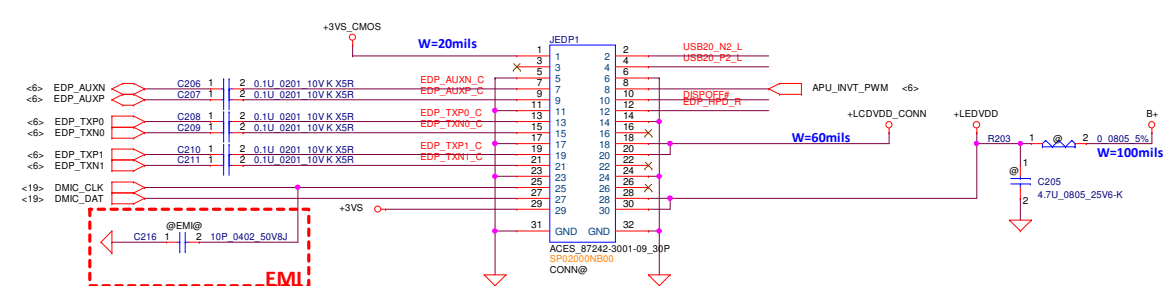
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Memory Partition A



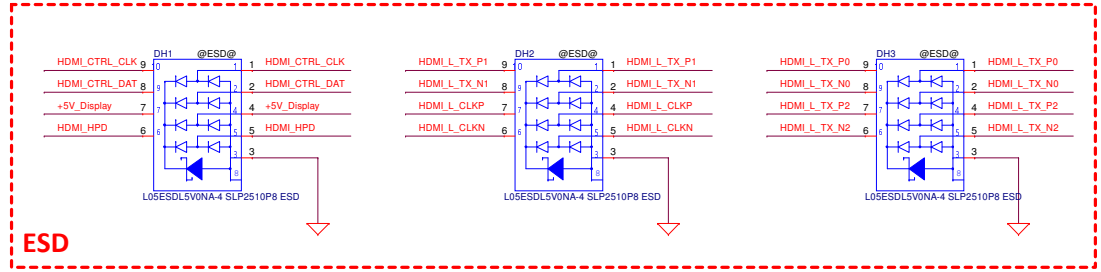
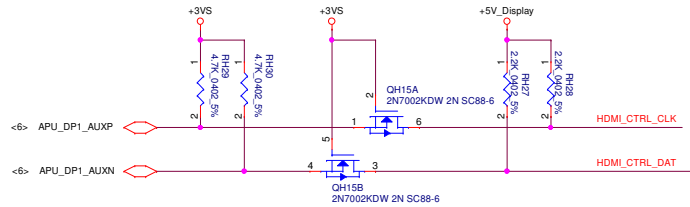
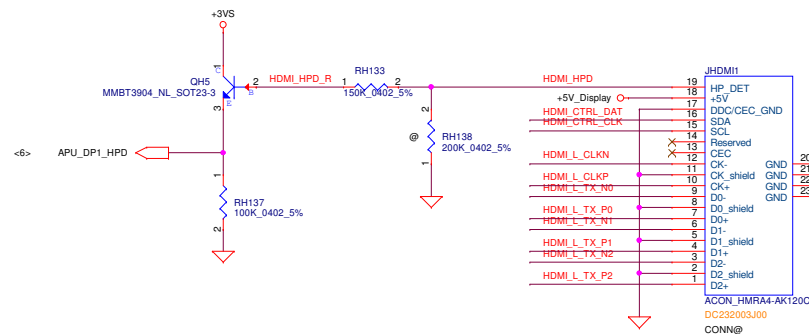
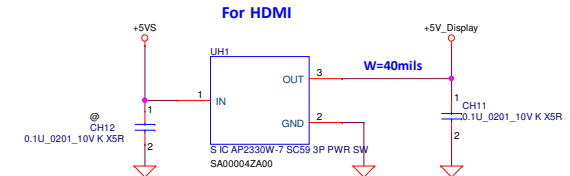
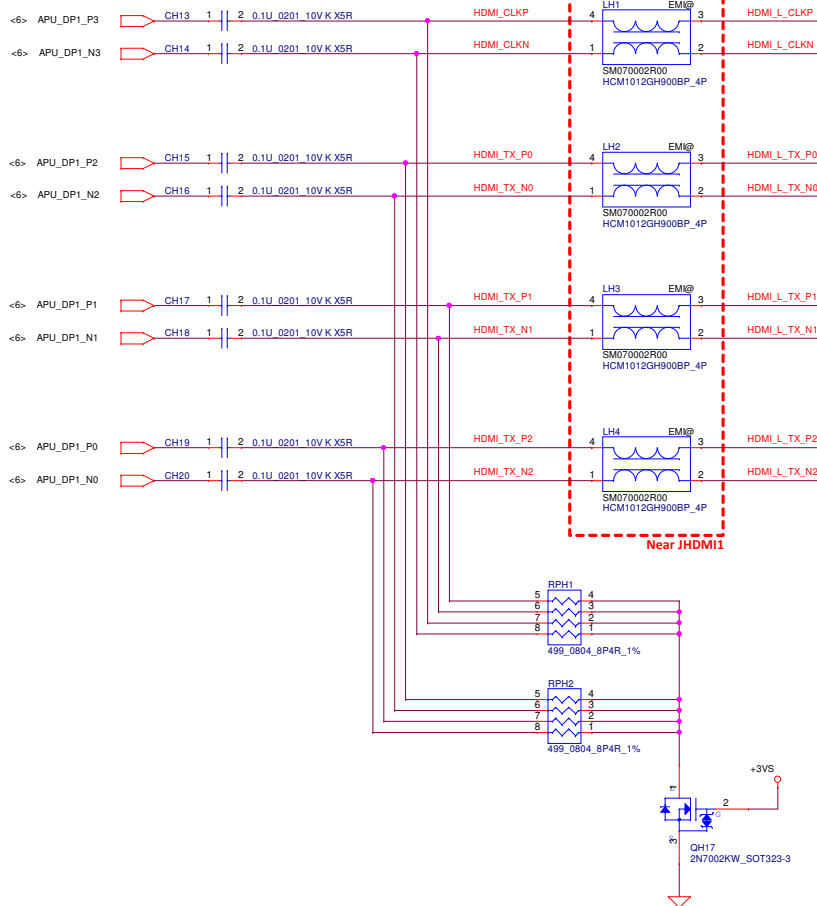


eDP CONN.



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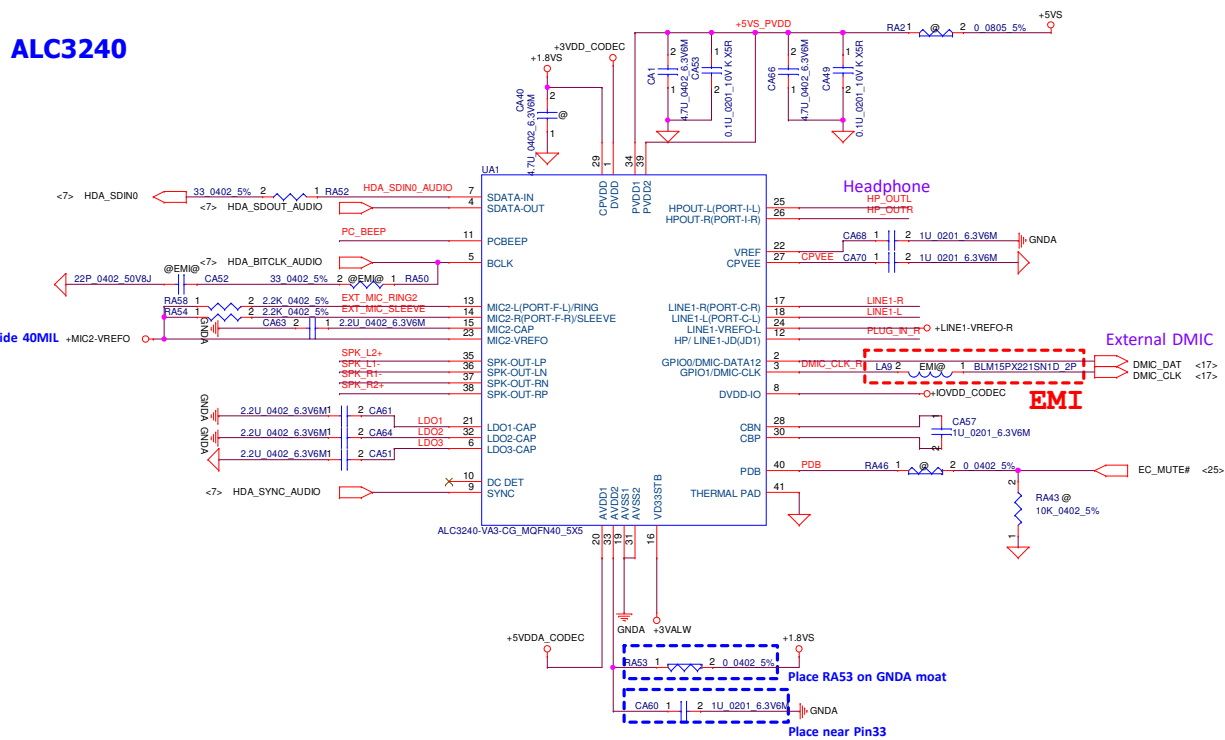
HDMI



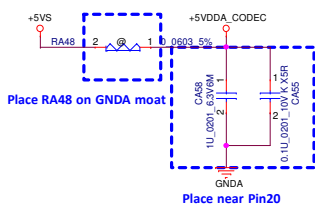
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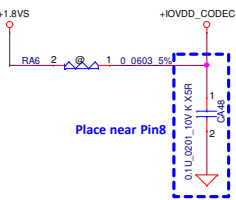
-5VS to
-5VDDA_CODEC



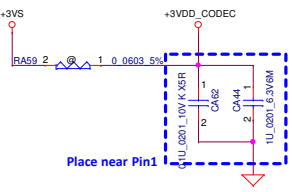
Each Platform HDA Link Voltage Support (Pin 7) :

	3.3V	1.8V	1.5V
AMD Carrizo-L			V
AMD Stoney Rade FT4		V	

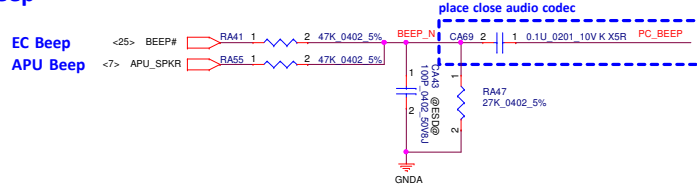
**+1.8VS to +IOVDD_CODEC
(For AMD FT4)**



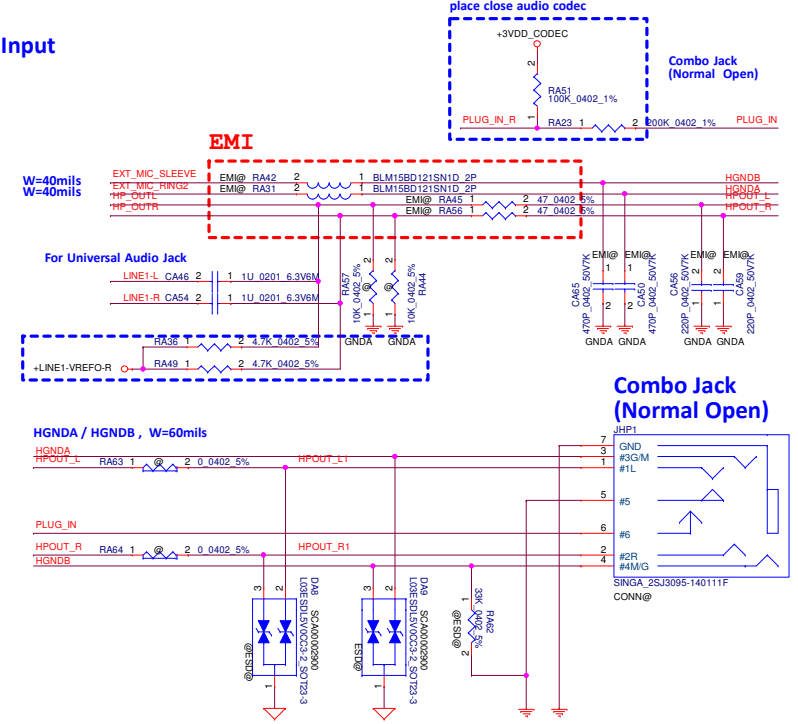
+3VS to +3VDD CODEC



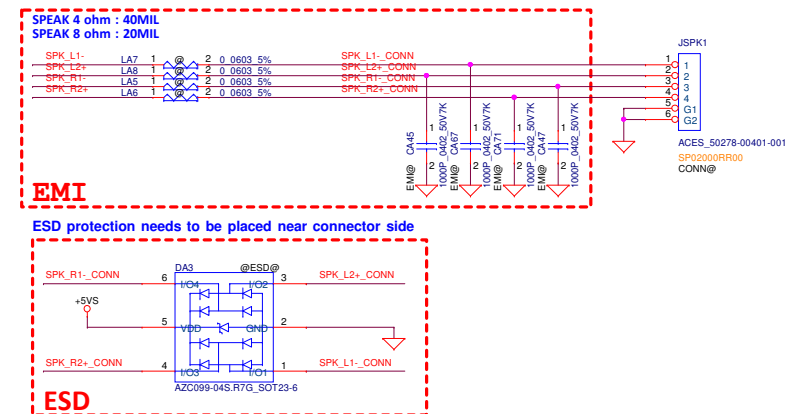
PC Beep



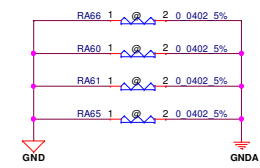
Input



Output

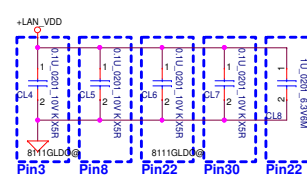
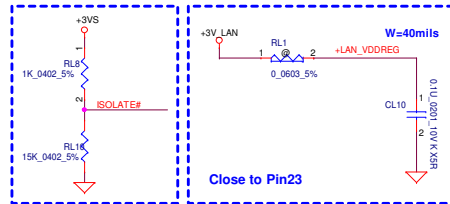
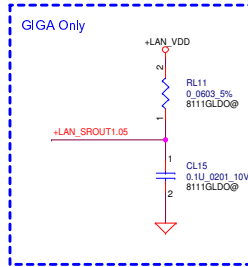
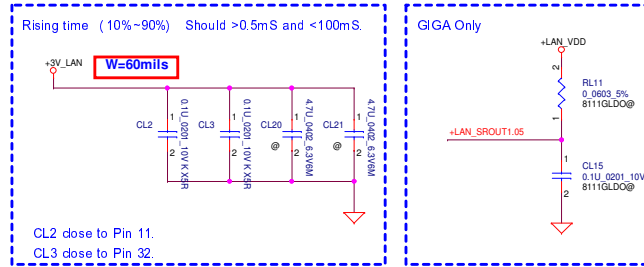
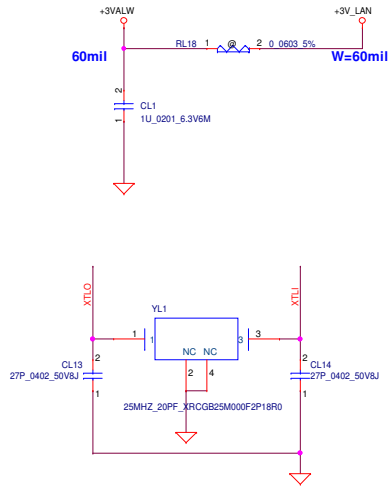


EMI

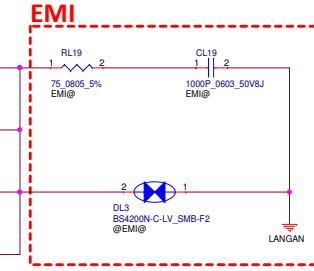
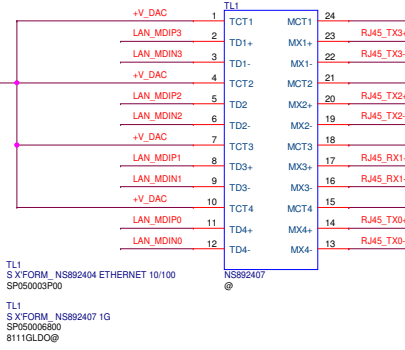
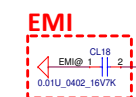
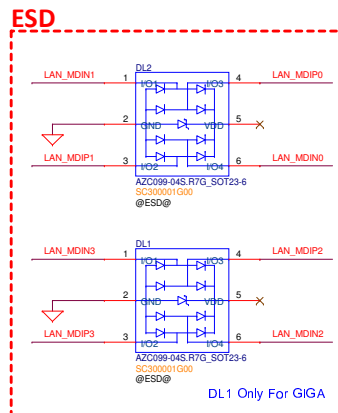
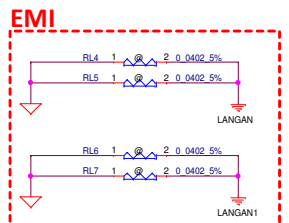
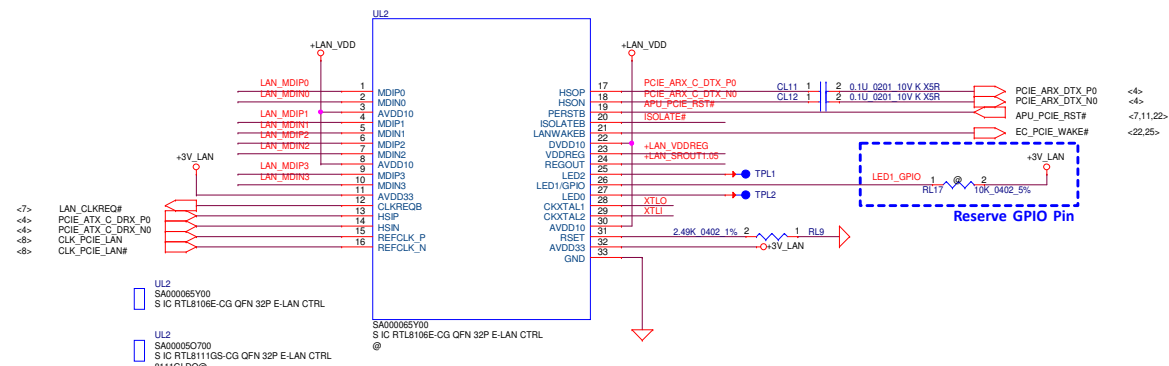
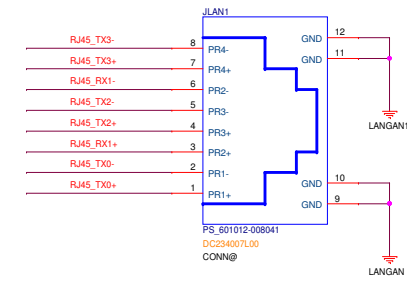


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				Size	Document	Number	Rev
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Date:				Monday, March 12, 2018		Sheet 19 of 43	

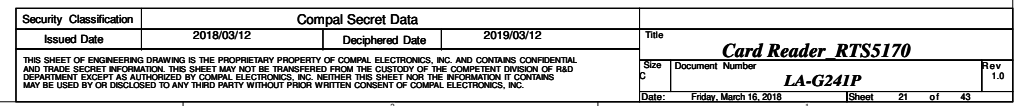
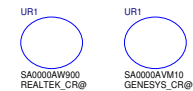
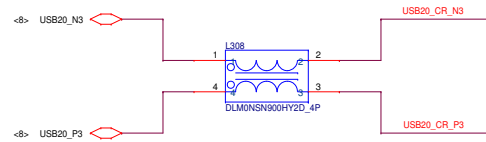
LAN



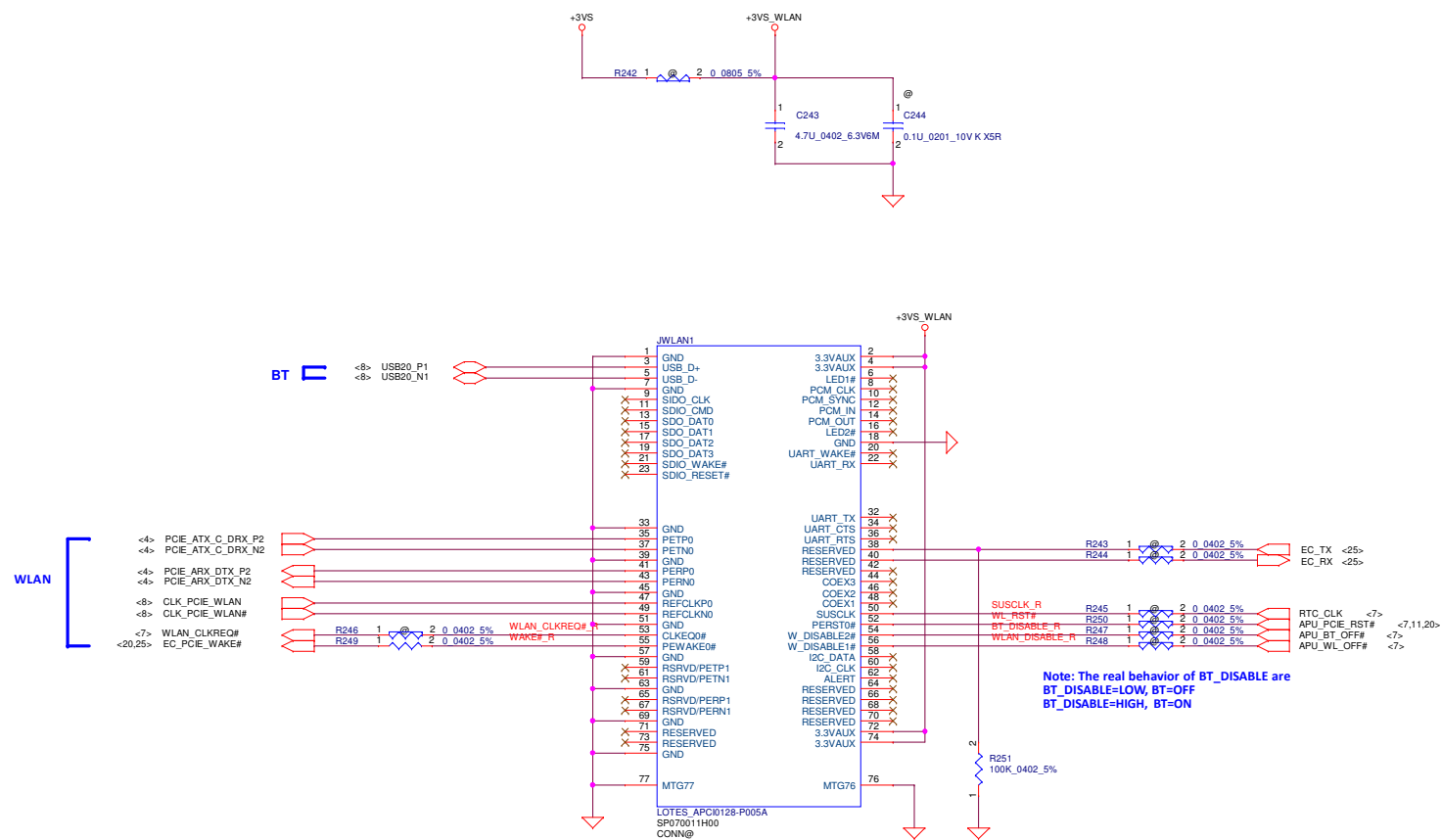
RJ-45 Connector



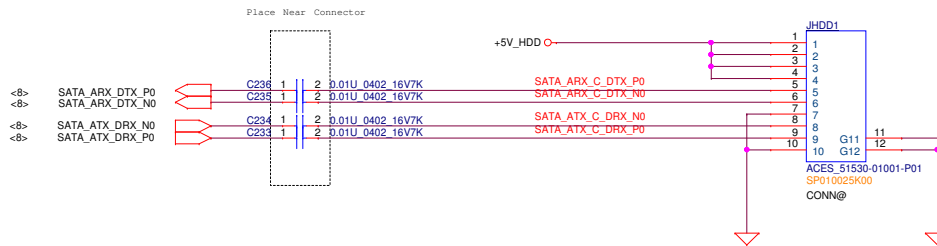
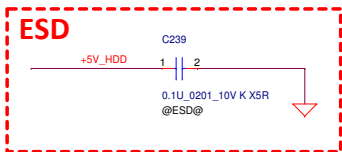
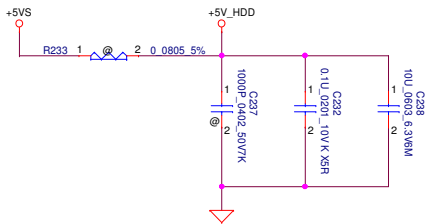
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Issued Date	2018/03/12	Deciphered Date
2019/03/12		
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		LAN RTL8111 / RTL8106
Size	Document Number	Rev
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NGFF - WLAN / BT (E- KEY)

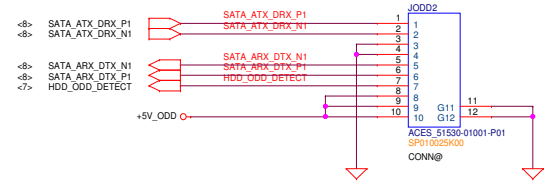


HDD FFC Connector to Sub Board

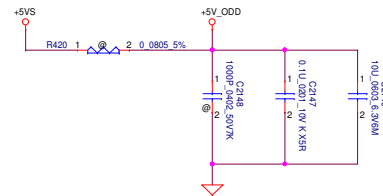


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Custom			1.0			
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ODD FFC Connector to Sub Board (15" Only)

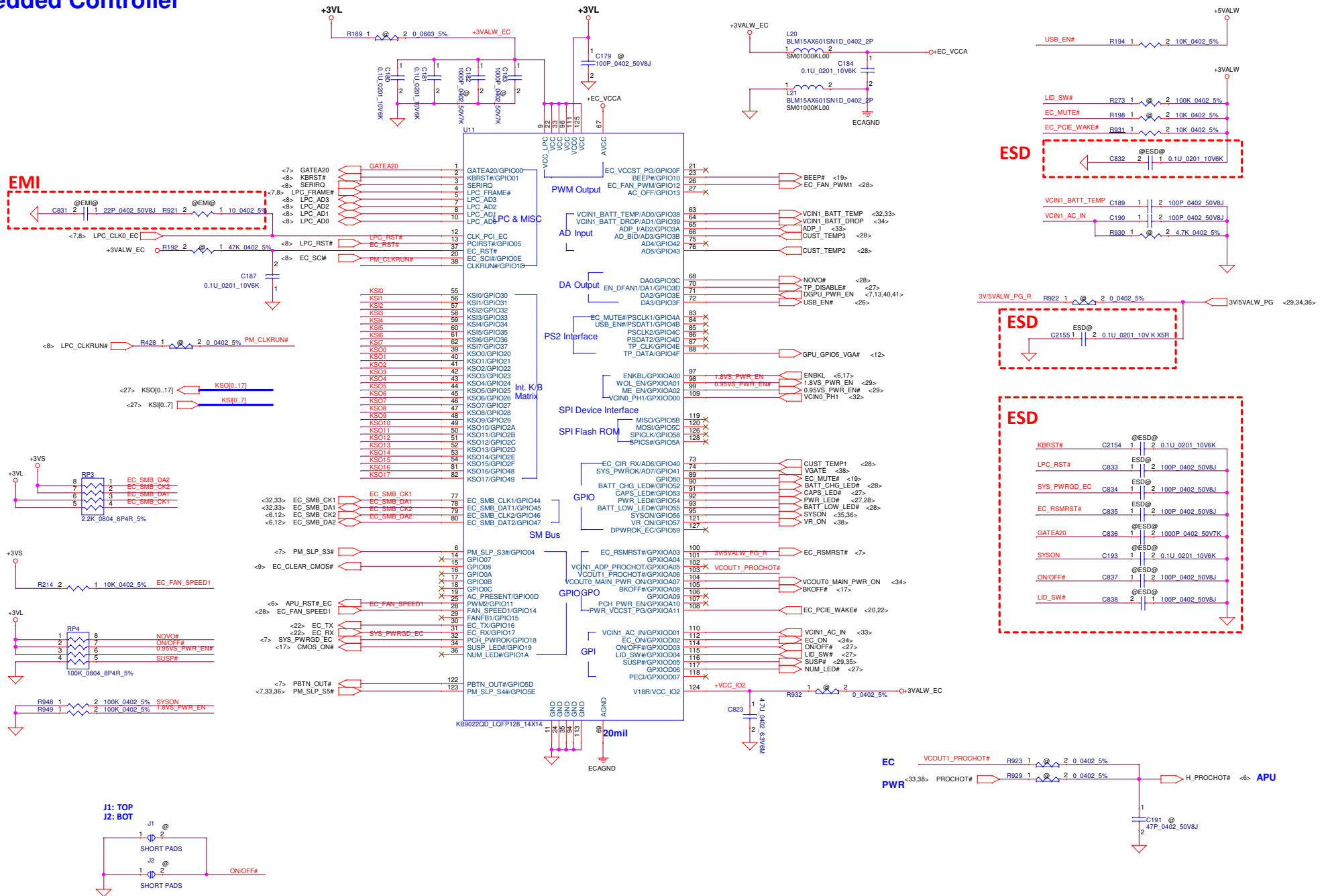


ODD MISC.



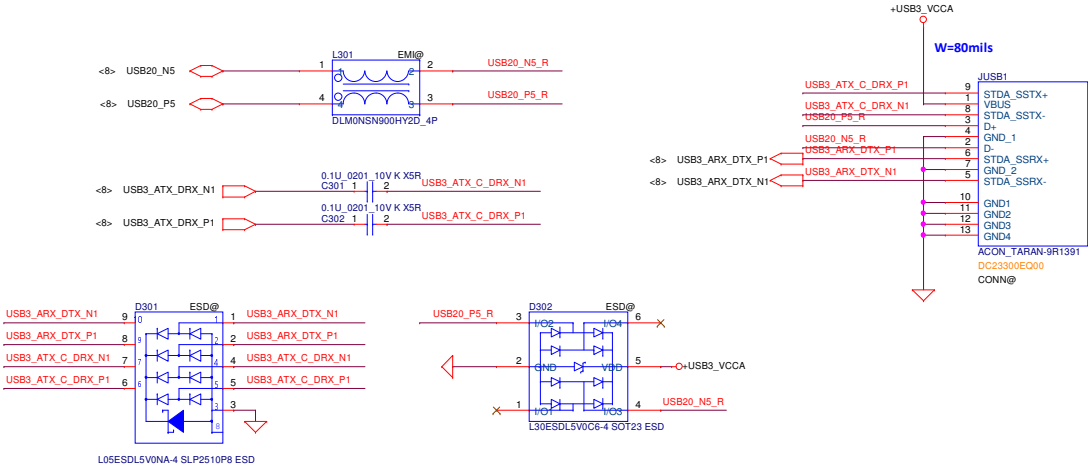
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Embedded Controller

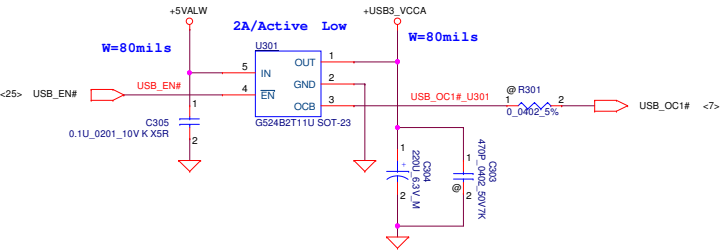
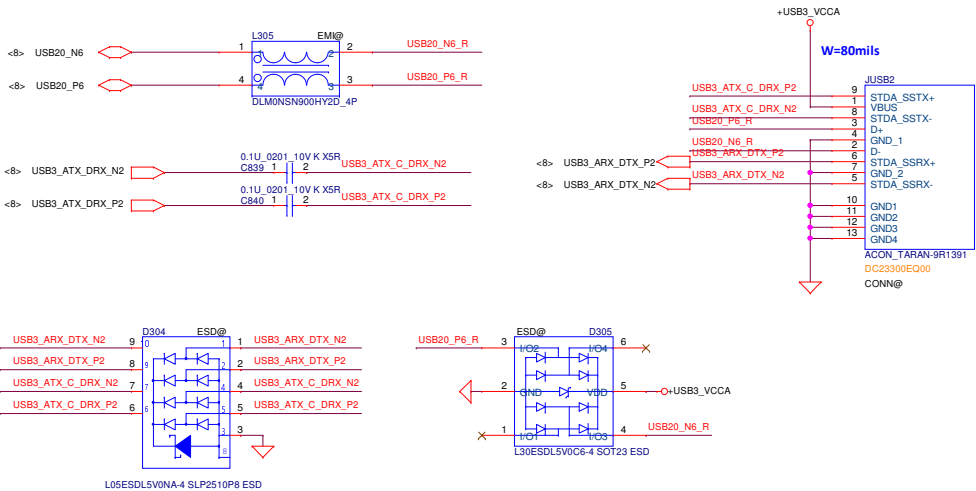


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USB 3.0 (PORT 1)

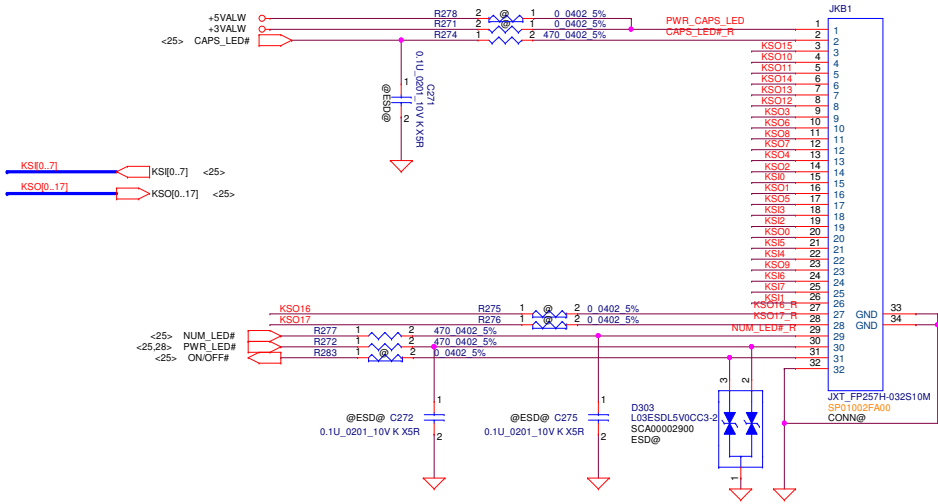


USB 3.0 (PORT 2)

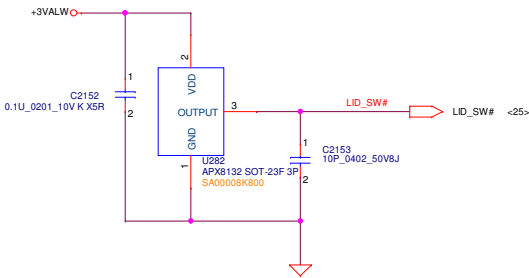


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Issued Date	2018/03/12	Deciphered Date	2019/03/12	Title	
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				Size	Document Number
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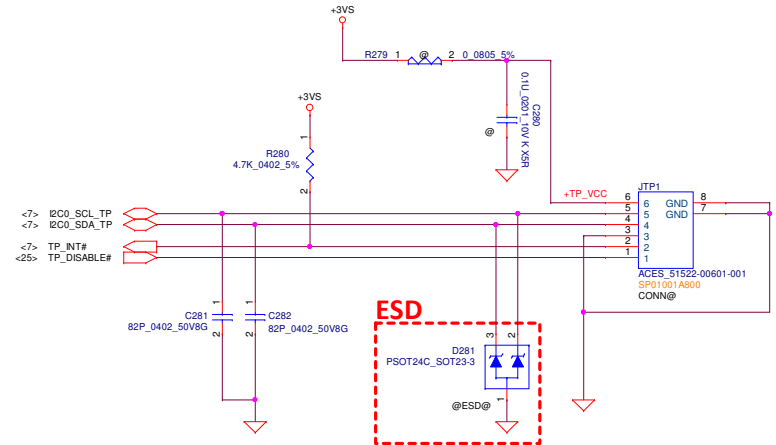
Keyboard



Hall Sensor



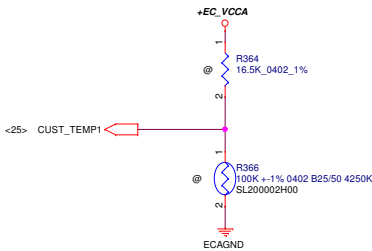
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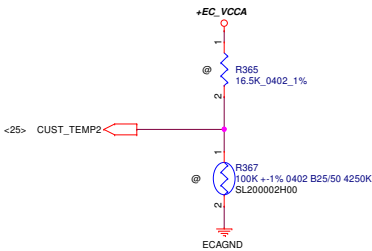
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Issued Date	2018/03/12	Deciphered Date	2019/03/12	KBD/Hall Sensor/TP	
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Thermal Diode

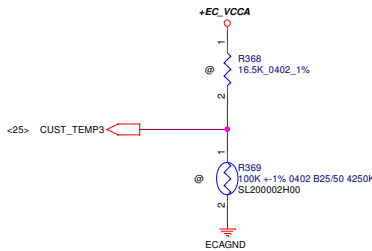
Batt Charge



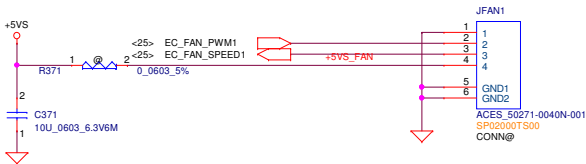
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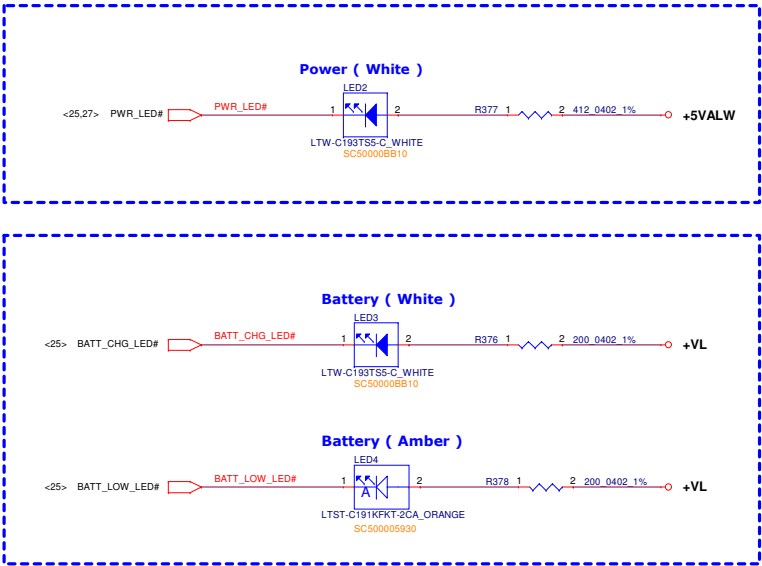
CPU Chock



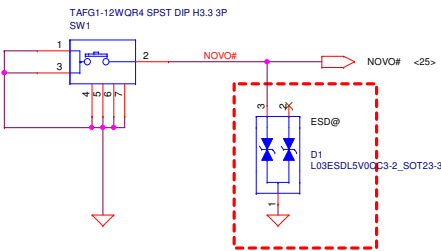
FAN



LED

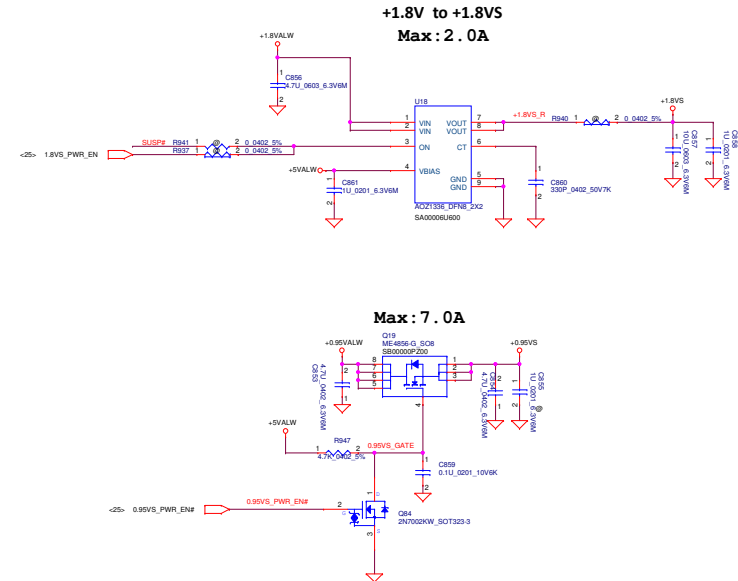
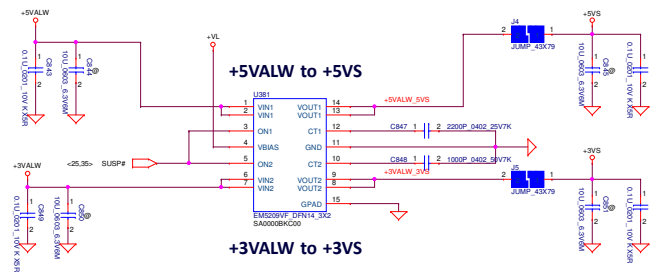


NOVO BUTTON

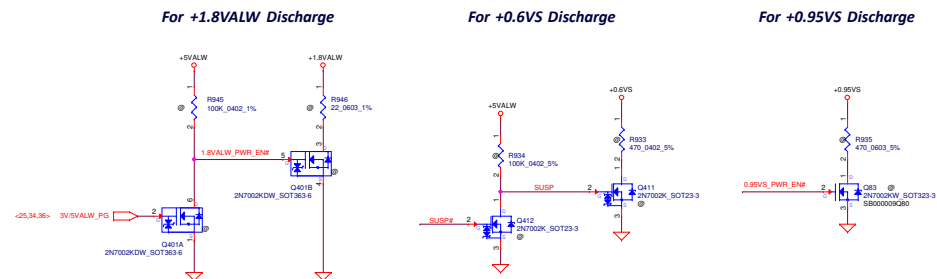


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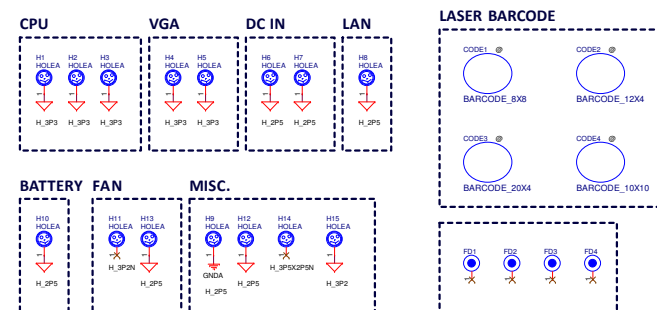
DC to DC



Discharge Circuit



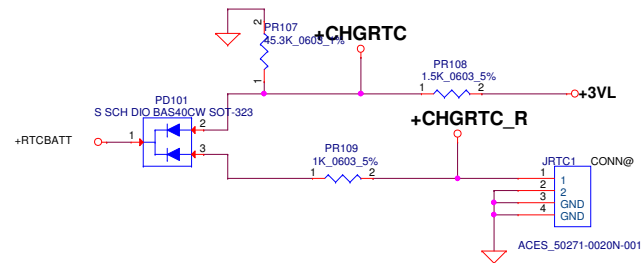
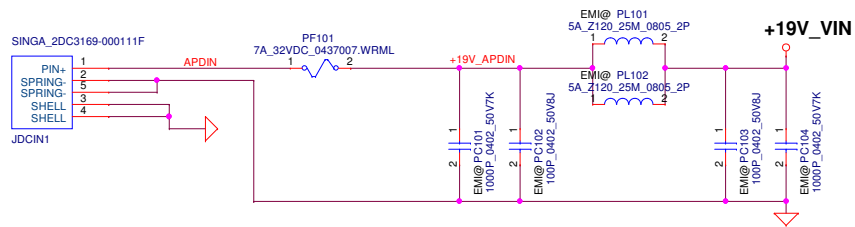
MISC.



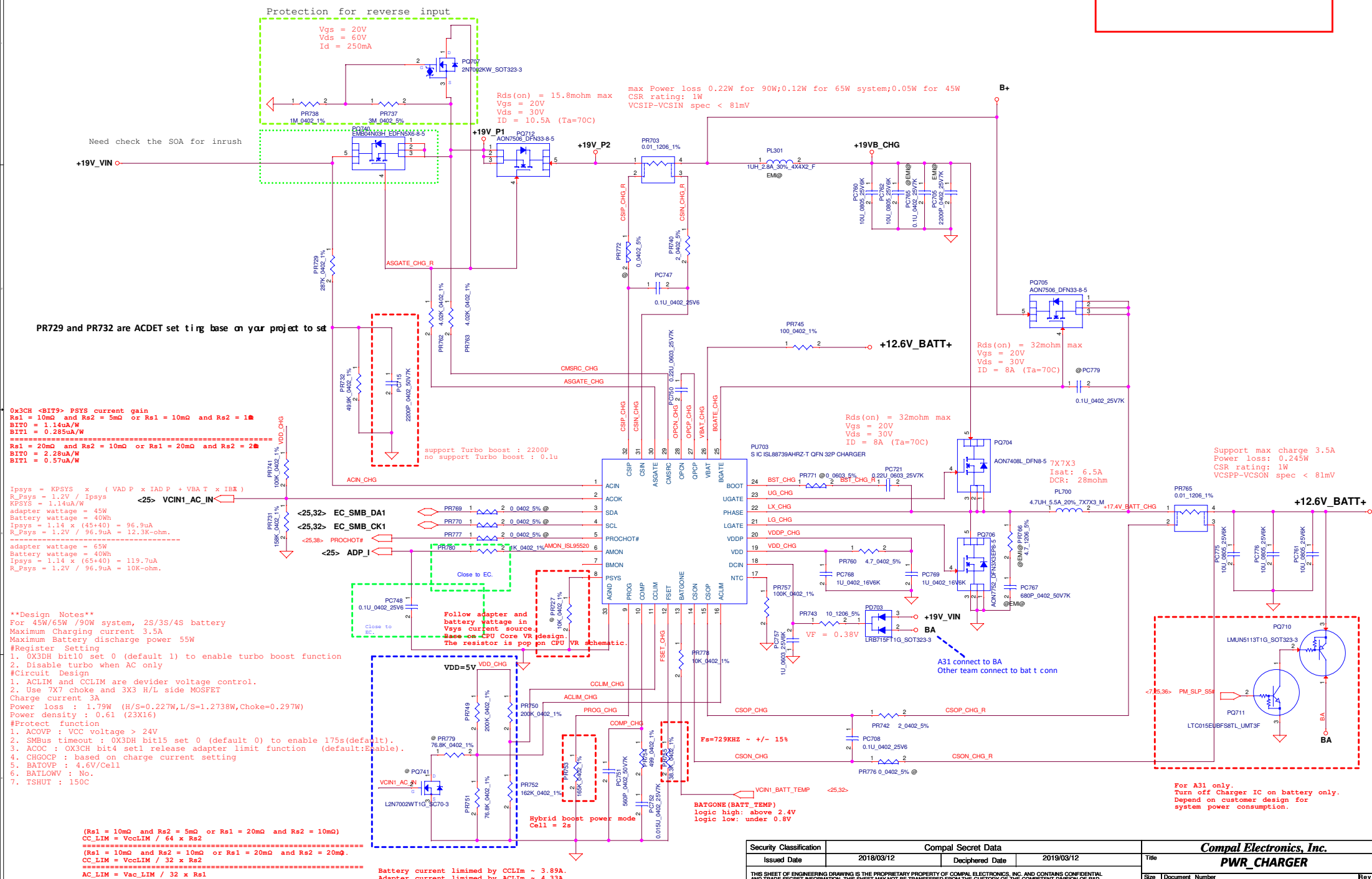
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Issued Date	2018/03/12	Deciphered Date	2019/03/12	DC to DC /Discharge /MISC	
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				Size Custom	Document Number
				LA-G241P	
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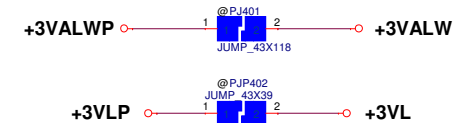


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Size	Document	Number	Rev	1.0	
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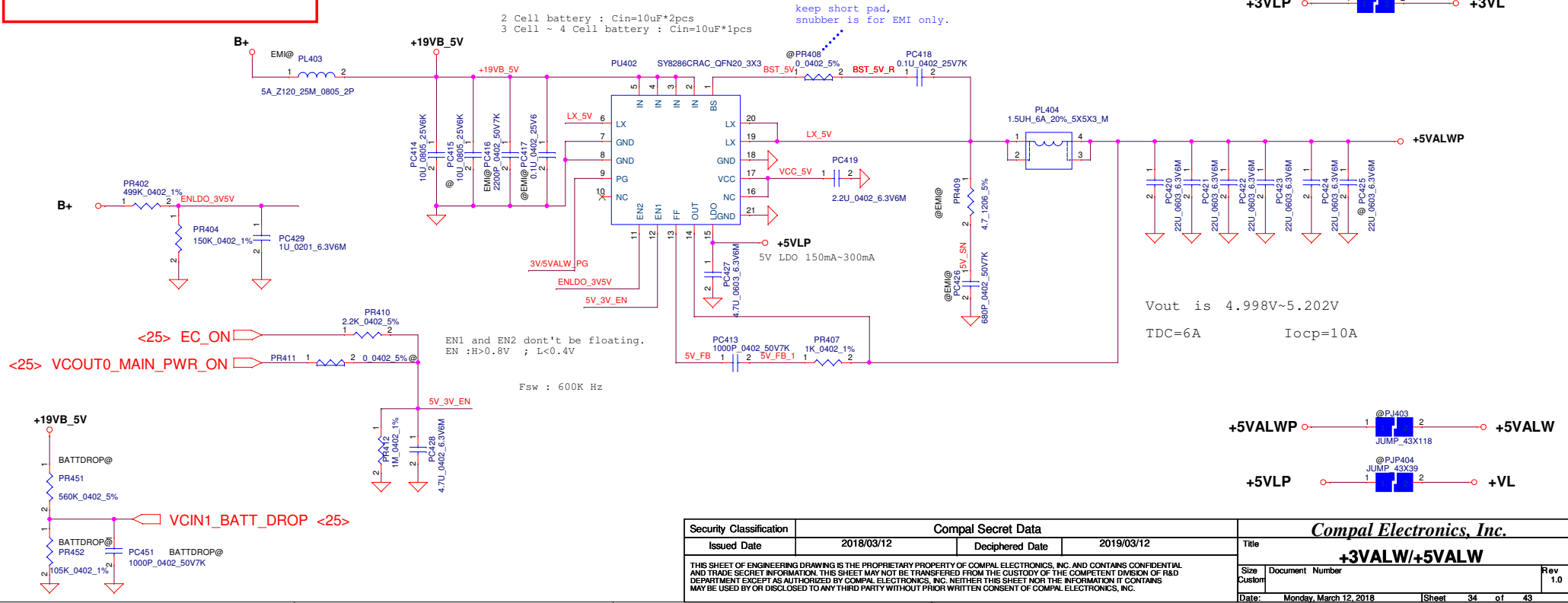


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SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd



SY8286C_V3_single.mdd
SY8286C_V3_dual.mdd

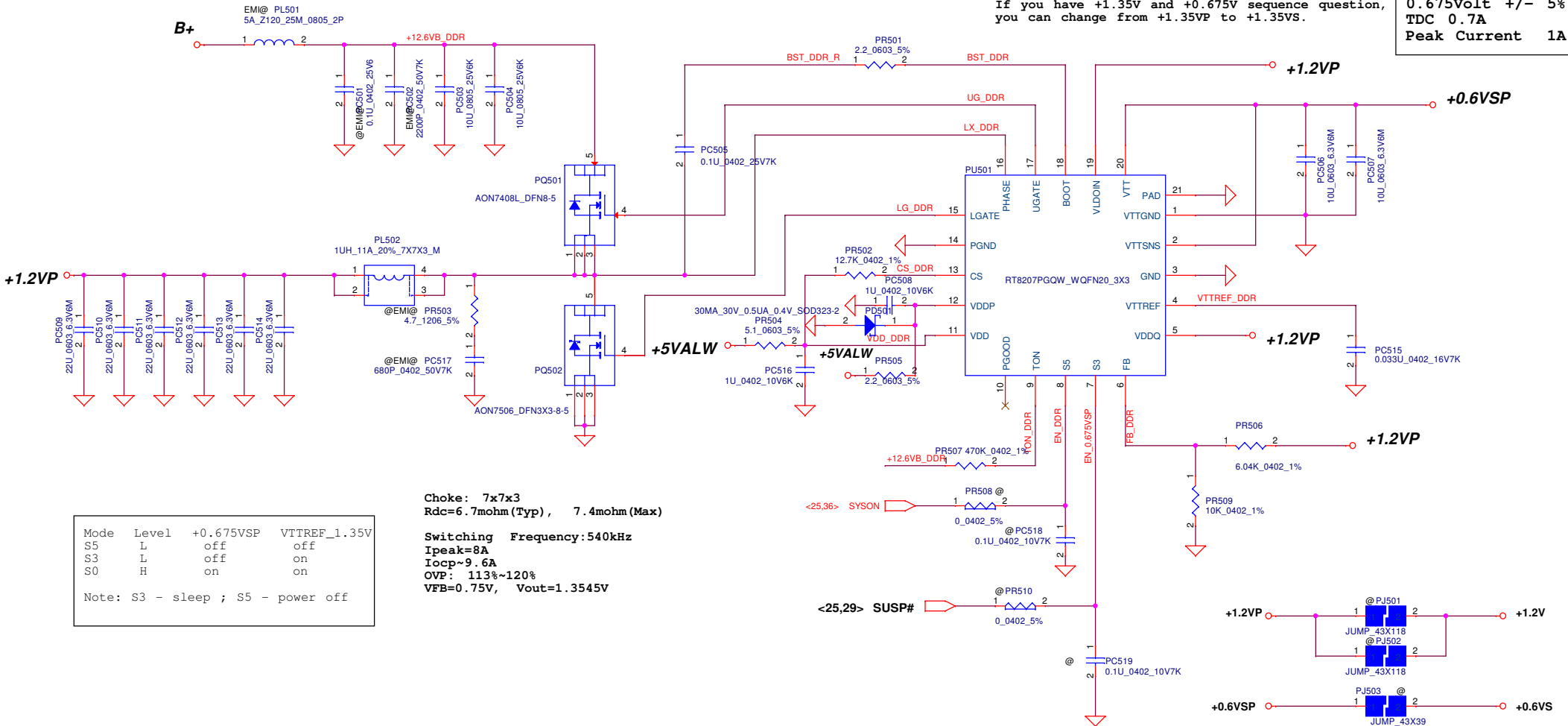


Module model information

RT8207P_single_V3.mdd For Single layer
RT8207P_dual_V3.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

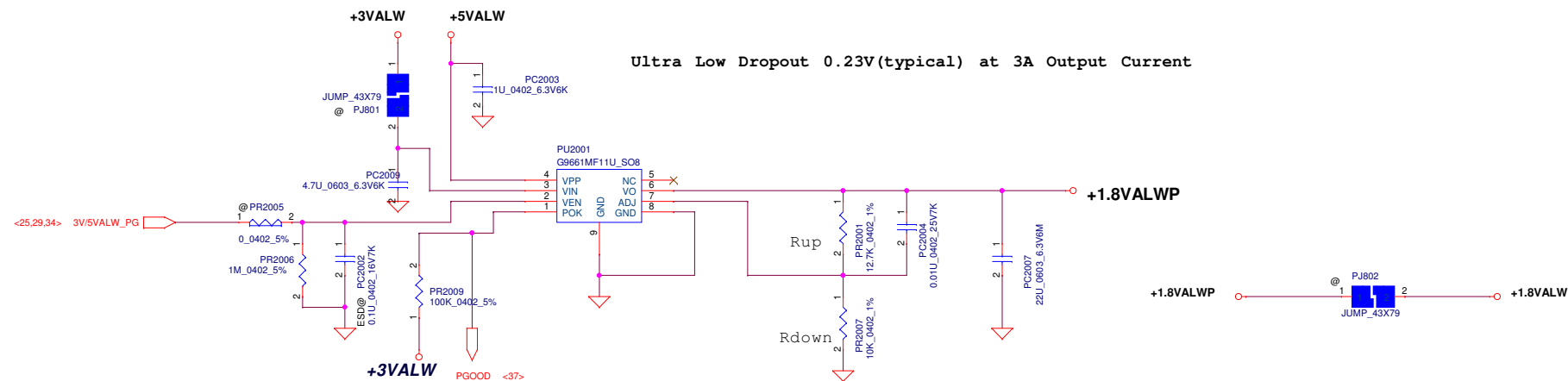
0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



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								Custom		1.0			
						Date:		Monday, March 12, 2018					
						Sheet		35 of 43					

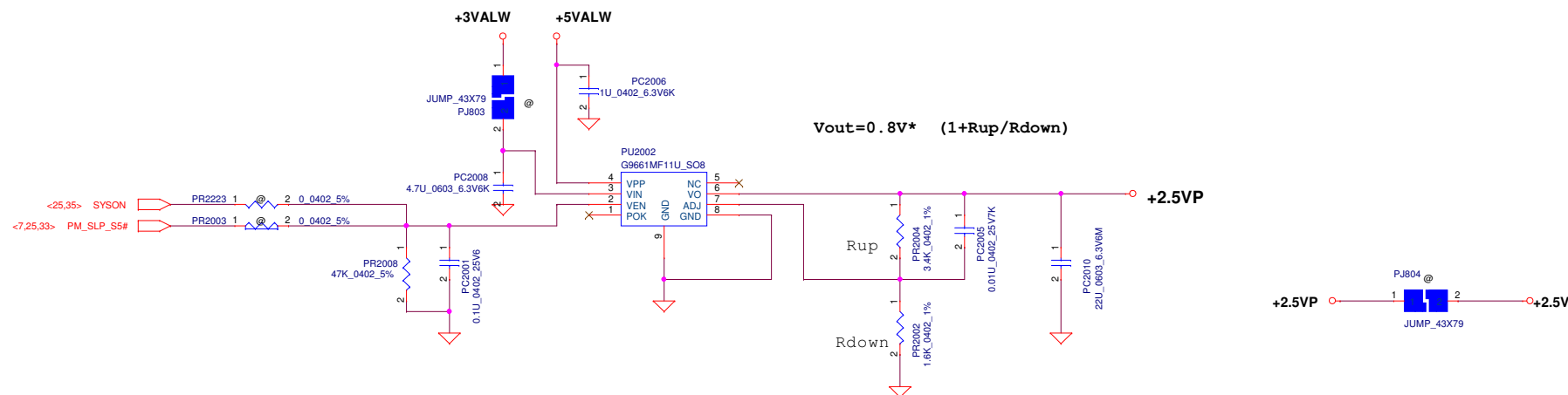
Module model information

APL5930_V2.mdd



$$V_{out} = 0.8V * (1 + R_{up}/R_{down})$$

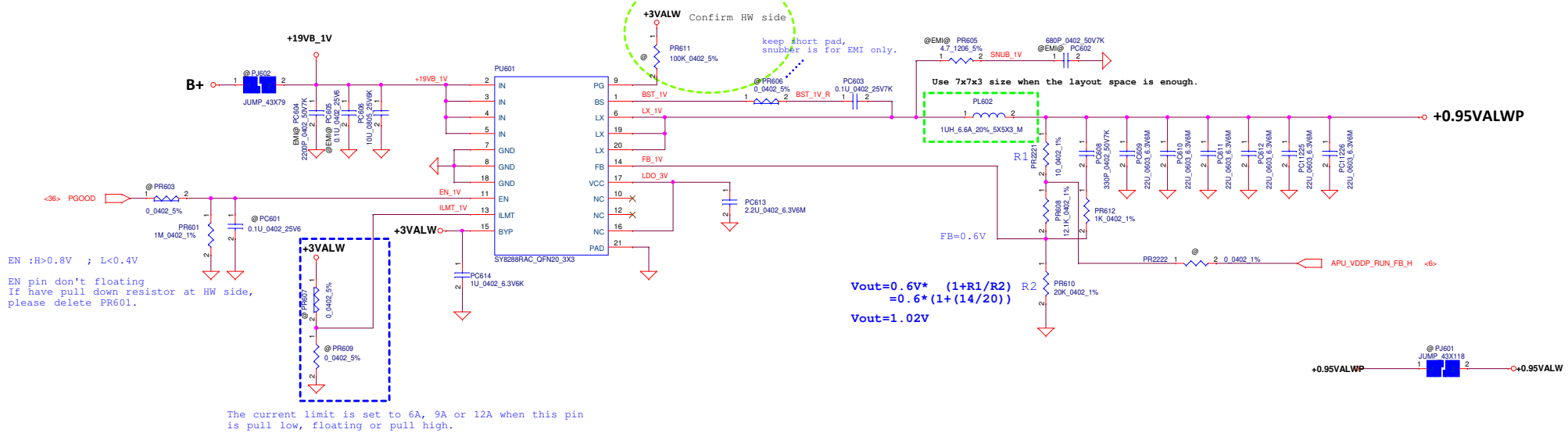
$$V_{out} = 0.8V * (1 + R_{up}/R_{down})$$



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				Rev	1.0
				Date:	Monday, March 12, 2018
				Sheet	36 of 43

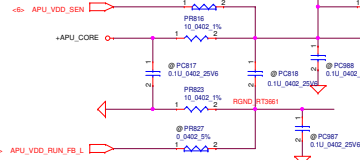
Module model information

SY8286_V2_single.mdd
SY8286_V2_dual.mdd



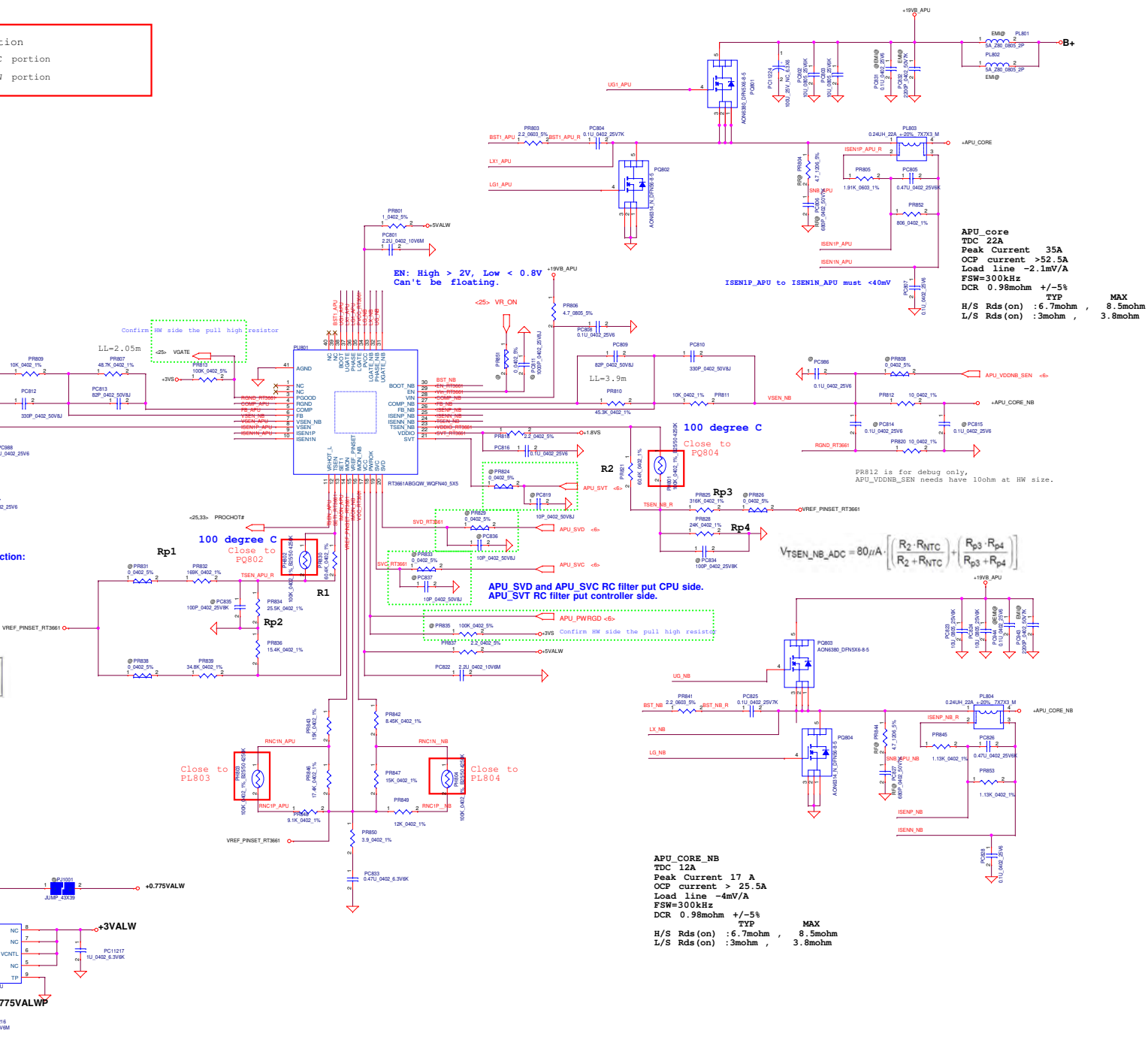
Module model information
RT3661AB_V2A.mdd for IC portion
RT3661AB_V2B.mdd for SW portion

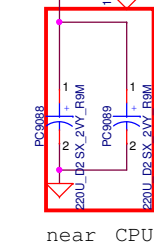
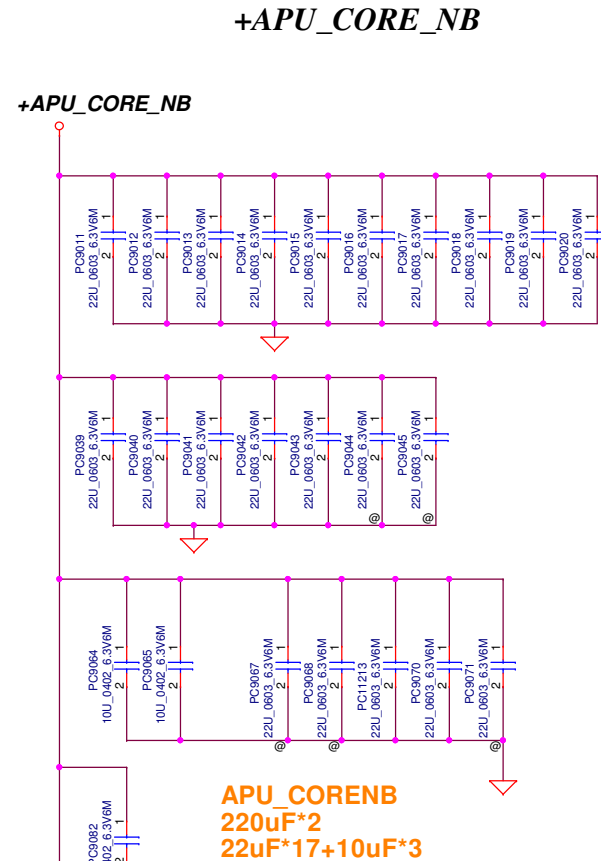
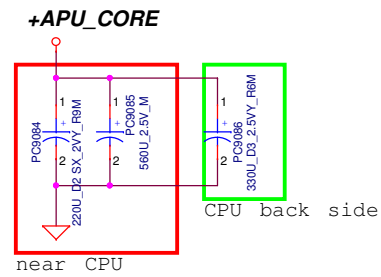
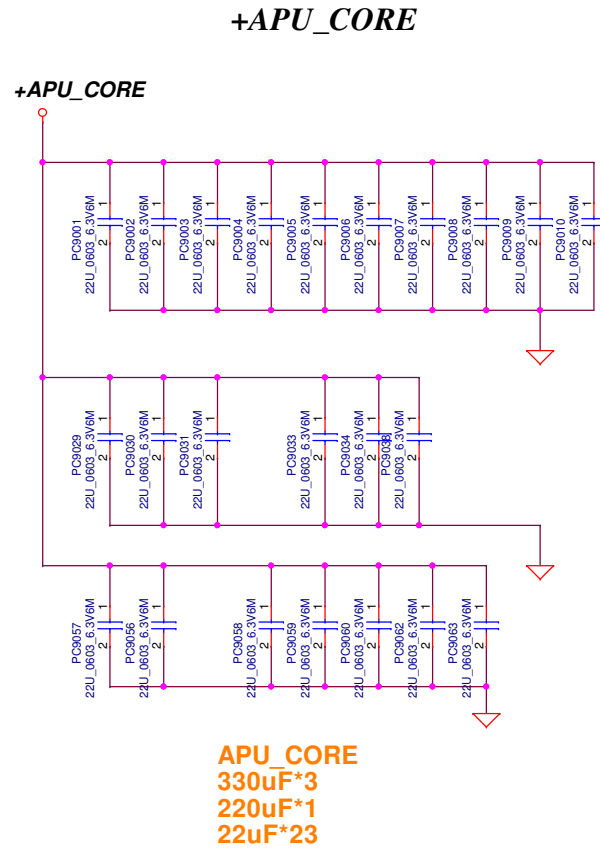
PR816, PR823 are for debug only,
APU_VDD_SEN, APU_VDD_RUN_FB_L need have 10ohm at HW size.



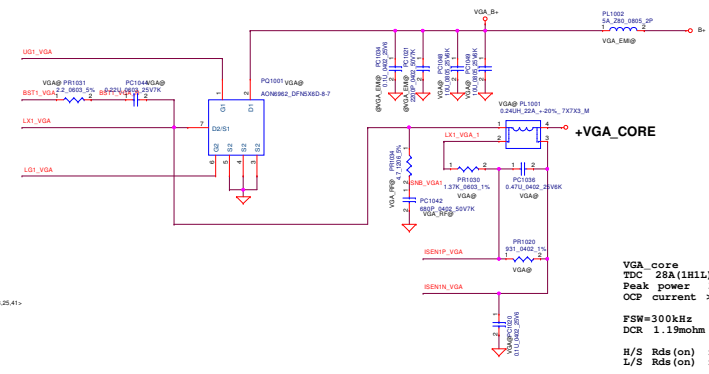
RT3661AB SET1, TSEN and TSEN_NB Pin Setting Function:
AI VDD=100%, AI VDDNB=100%
OR Threshold: Disable
Frequency: 300kHz
VDD and VDDNB Initial Offset: 0mV (PS0)
VDD and VDDNB PHOCSET Setting Ratio: 150%

$$V_{TSEN_ADC} = 80 \mu A \cdot \left[\frac{R_1 \cdot R_{NTC}}{R_1 + R_{NTC}} + \frac{R_{p1} \cdot R_{p2}}{R_{p1} + R_{p2}} \right]$$



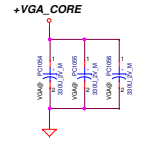


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Custom	LA-G241P				
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VGA_core
TDC 28A(1H1L)
Peak power 38W
OCP current > 40A

FSW=300kHz
DCR 1.19mohm +/-5%
          TYP
H/S Rds(on) : 6.8mohm , 8.6mohm
L/S Rds(on) : 2.0mohm , 2.5mohm
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